MAINTENANCE MANUAL

FOR THE

3600 SERIES INTECOLOR TERMINALS

AND

DESKTOP COMPUTERS
(including Compucolor II)

999300 01/04/85

WARNING !

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. Equipment of current manufacture has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. 3600 Series equipment of early manufacture and Compucolor II, as then temporarily permitted by regulation, were not so tested for compliance. Operation of this equipment, of either current or early manufacture, in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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IMPORTANT NOTICE

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DEFINITIONS

WARNING!

Where the word **WARNING!** is used in this manual, the associated note refers to operations or procedures which involve possible exposure to dangerous voltages, contact with which could result in personal injury or even death.

CAUTION!

Where the word **CAUTION!** is used in this manual, the associated note refers to operations or procedures which involve possible damage to equipment.

TRAINED AND QUALIFIED

Where the words PERSONS TRAINED AND QUALIFIED are used in this manual, they refer to either of two types of individuals:

1) Persons who through general technical training are aware of the possible dangers in working in proximity to hazardous voltages and know how to avoid personal injury in working with equipment involving safety hazards.

or

2) Persons who have received specific training in use of the procedures involved and in the safe performance of these procedures.

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SECTION I

GENERAL DESCRIPTION

SECTION I. GENERAL DESCRIPTION

The 3600 Series of Intecolor desktop units includes data handling and processing devices that can function as complete stand-alone computer systems or as an interactive intelligent data terminals. Each system, including a keyboard (and a Mini-disk drive in some configurations), is housed in a single attractively-styled molded cabinet.

All units in the 3600 Series feature color graphics on a 128 x 128 grid. The dispaly format for standard characters is 32 lines with 64 characters per line. Each unit in the series has a standard 13" color CRT which can display any of eight foreground and eight background colors -- red, blue, green, yellow, magenta, cyan, black and white. Product current in 1984 uses the pre-converged in-line CRT. In older product, excellent convergence is readily obtained with nine-sector control from a recessed front panel.

The basic 3601 Terminal includes an Analog module which generates the system low voltages and line-frequency sync, the regulated high voltages and bias voltages for the CRT, and the horizontal sweep, vertical sweep and convergence waveforms. A small Video Driver module is mated to the CRT base. The Digital (Logic) module includes circuits for the microcomputer, the display generator and display memory functions. RS-232-C compatible serial I/O is available via a 25-pin connector at the rear of the console. User-designed and furnished interfacing for additional I/O or other devices is possible via a 50-pin bus, also at the rear of the console.

In the 3650 Series of computers the Logic module also includes disk drive control and interfacing for handling both 5.25" Mini-disk and 8" Floppy Disk drives -- either single or dual headed. In addition to the RS-232-C compatible serial I/O, the 3650 Series units have an X-Bus with 8-bit parallel I/O, six address bits, XI/OR and XI/OW. All X-Bus lines are buffered. If a 50-pin edge connector is used, the remaining 10 address bits and certain other signals (all unbuffered) are available for user implementation.

The full-size built-in keyboard is available in three versions: the standard 72-key, including cursor controls; the 101-key version, which has numeric and color clusters added; and the 117-key keyboard, which has 16 plot/function keys as well.

Standard units in the 3600 Series have included the:

Intecolor 3601 Terminal with 72-key Keyboard
Intecolor 3621 Computer with 117-key Keyboard, 32K of User RAM and an external Micro-Disk Drive
Intecolor 3651 Computer with 72-key Keyboard, an internal Mini-Disk Drive and 16K of User RAM (optionally 32K)
Intecolor 3652 Computer, similar to the 3651 but with two Mini-Disk Drives
Intecolor 3653 and 3654 Computers with dual 8" Floppy Disk Drives, single head and double head respectively

Other 3600 Series units have been manufactured. A number of options are available.

In order to keep maintenance information available for the Compucolor II, manufacture of which has been discontinued, its specifications, alignment procedure, circuit descriptions and schematics have been included in this manual.

The Compucolor II used the same 64 character by 32 line format as the 3600 Series units. Operation was much the same as for the 3621. The Logic Module, Microdisk Drive and Keyboard of the 3621 are much the same as those in the Compucolor II. Circuit differences were in the analog and video driver areas.

Components were housed in a television-type cabinet. Display was on a 13" diagonal in-line (but not preconverged) color CRT. The keyboard was separate. There was provision for one or two microdisk drives.

Specifications, installation information, alignment procedures and circuit descriptions are included at the ends of Sections II, III, IV and V respectively. Schematic drawings are near the end of the Drawings section.

SECTION II

SPECIFICATIONS

II. SPECIFICATIONS

Intecolor 3600 Series Specifications

Operating Conditions

Power	105-125 volts, 50/60 Hz., 100 to 150 watts. (Optionally 210-250 VAC)
Temperature	+10°C to +40°C Operating -30°C to +70°C for storage only
Humidity	0 to 95% non-condensing

Physical Dimensions

Cabinet size	19 3/4" W x 13 3/4" H x 26 5/8" D
Weight	51 pounds
Shipping Weight	62 pounds
Micro-Disk Drive	5 7/8" W x 3 1/2" H x 8 1/4" D, 4 pounds
Mini-Disk Drive	
Single	6" W x 3 3/4" H x 12 1/2" D, 8 pounds
Dual	11 3/4" W x 3 3/4" H x 12 1/2" D, 16 pounds
8" Floppy Disk Drive	
Single	9" W x 6" H x 20" D, 25 pounds
Dual	21" W x 5 1/2" H x 23 1/2" D, 48 pounds

Display

CRT Type	13-inch diagonal, 90 square inches in area. Pre-converged in-line. (Older units have standard resolution delta gun or optional high phosphor density delta gun).
Colors	Eight colors, background and foreground (red, green, blue, yellow, magenta, cyan, black and white).
Dimensions	9.5" wide x 7.25" high, 4 x 3 aspect ratio.
Format	64 characters per line, 32 lines per page (or 16 lines with 2X character height).
Characters	64 ASCII characters, 5 x 7 dot matrix within a 6 x 8 dot pattern, plus 64 special characters in a 6 x 8 matrix. (Other character sets available as options.) 128 x 128 graphics and vector generating software.

Cursor	White blinking underscore in 3650 Series, overscore and underscore in other units, non-destructive.
Refresh rate	60 or 50 times per second, synchronized to power line frequency.

Keyboard

Type	72 gold crossbar commercial key switches. Coded with 192 codes. (Optionally 101 keys or 117 keys -- 117-key option provides 256 codes).
Features	Cursor controls, CPU Reset, Erase Line, Erase Page. (101-key option adds 16-key number/mathematics pad, 9-key color/command pad and 4 other function keys; 117-key option further adds 16 plot/function keys.)

Microcomputer

CPU	8080 2-microsecond CPU with total address capability of 64K.
Memory	16K bytes of non-destructive read only memory (ROM). (Optional add-on board has four sockets for additional ROM, up to 8K) 4K bytes of random access memory (RAM) for CRT screen refresh. 3650 Series units have 4K bytes of RAM for disk buffer. User dynamic RAM to 32K bytes in computer configurations. 16K standard in 3650 Series, with additional 16K optional. 32K standard in 3621. 3601 has 128 bytes of static RAM for terminal operations.
I/O Ports	One RS-232-C serial asynchronous channel for a modem or printer. Other ports available for user implementation via 50-pin bus. Baud rate is keyboard selectable for one of seven rates, ranging from 110 baud to 9600 baud. One or two stop bits. No parity. 3650 Series has disk drive I/O capable of supporting up to three 5.25" Mini-Disk Drives and four 8" Floppy Disk Drives, single or double headed. The 3650 Series also has an X-Bus for 8-bit parallel I/O.

Editing	Page Roll Mode, Erase Line, Erase Page, Tab, Caps Lock, CPU Reset and Color Selection.
Language	Intecolor 3650 Series and the 3621 have Extended Disk BASIC interpreter in ROM which includes 27 statement types: CLEAR, DATA, DEF, DIM, END, FILE, FOR, GET, GOSUB, GOTO, IF, INPUT, NEXT, ON, OUT, PLOT, POKE, PRINT, PUT, READ, REM, RETURN, RESTORE, STEP, THEN, TO and WAIT. Five command types: CONT, LIST, LOAD, RUN and SAVE. 18 mathematical functions: ABS(x), ATN(x), CALL(x), COS(x), EXP(x), FRE(x), INT(x), INP(x), LOG(x), PEEK(x), POS(x), RND(x), SGN(x), SIN(x), SPC(x), SQR(x), TAB(x) and TAN(x). Nine string functions: ASC(x$), CHR$(x), FRE(x$), LEFT$(x$,I), LEN(x$), MID$(x$,I,J), RIGHT$(x$,I), STR$(x) and VAL(x$). Disk File commands: COPY, DEVICE, DIRECTORY, INITIALIZE, LOAD, PRINT, READ, RENAME, RUN, SAVE and WRITE. The 3621 Intecolor also includes FORTRAN.

Disk Drives - 3650 Series

Medium	5.25" Sof-disk using 40 tracks, 18 sectors 8.00" Sof-disk using 77 tracks, 30 sectors
Capacity	Accessible with disk(s) in drive(s), Single Mini-Disk Drive — 92,160 bytes Dual Mini-Disk Drive — 184,320 bytes Dual 8" Floppy Disk — 295,680 bytes Dual Double Headed 8" — 591,360 bytes
Data Transfer	125 Kilobits per second in 5.25" drives and 250 Kilobits per second in 8" drives. The 5.25" drive requires approximately one second for speed stabilization.
3651 Intecolor	One built-in 5.25" single headed disk drive.
3652 Intecolor	One built-in and one external 5.25" single headed disk drives. The external drive has a separate power cord.
3653 Intecolor	External dual 8" single headed disk drives.
3654 Intecolor	External dual 8" double headed disk drives.

Disk Drives -- 3621 Computer

Medium	5.25" Sof-disk, using 40 tracks with a track density of 48 tpi.
Capacity	51.2K bytes per side. Both sides usable by flipping disk over.
Data Transfer	76.8 Kilobits per second. Average access time 400 milliseconds. Average latency 200 milliseconds.

Compucolor II Specifications

Operating Conditions:		As for the 3600 Series.
Physical Dimensions :		Cabinet 18.0" W x 13.6" H x 15.8" D Keyboard 18.7" W x 2.8" H x 6.9" D Weight 37 pounds, including keyboard Ship. Wt. 45 pounds complete
Display	:	13 inch diagonal in-line color CRT (not preconverged). 90 square inches in area, with display about 60 square inches. Colors, dimensions, format, characters, cursor and refresh rate as for the 3600 Series.
Keyboard	:	As for the 3600 Series.
Microcomputer	:	User RAM configured as 8K, 16K or 32K. Other factors as in the 3621 model, except Fortran is not included.
Disk Drives	:	As for the 3621 model.

SECTION III

INSTALLATION AND POWER-UP

III. INSTALLATION AND POWER-UP

General Considerations

The console portion of the 3600 Series unit should always by checked first on receipt. External disk drives and other devices should not be connected to the unit until proper operation of the console has been verified.

A 3600 Series Intecolor computer or terminal is intended for use on a desk or table or any similar vibration free horizontal surface that is free from dust and lint.

A space 20 inches wide by 28 inches deep is adequate for the console. Allow for 15 inches in height. The external disk drives of the 3652, 3653,3654 and 3621 can be placed at a convenient location nearby.

The unit may be used under normal room lighting conditions, but direct sunlight and excessively bright room lighting should be avoided (as would be the case for a color television set).

It may be installed adjacent to most types of electrical or electronic equipment, provided that it is not located within a strong magnetic field. (Operation within a strong magnetic field may affect the quality of the display and the transfer of data to or from the micro-disk drive unit in a 3621.)

No special cooling provisions need be made for the 3600 Series Intecolor unit, but there must be free flow of air around the console and the vents in the bottom of the cabinet must not be blocked.

Except for external disk drives and other optional peripheral devices, the only external connection is the 7-foot 3-wire power cord to a source of 115 VAC power.

Turn-on and Initial Test

For initial test of the 3600 Series Intecolor unit, proceed as follows.

Prior to power-up, use a small wire jumper to connect terminals 2 and 3 of the 25-pin MODEM socket at the rear of the console. (As viewed from the rear, these are the second and third from the right in the top row of socket terminals.)

Then connect the unit to a source of 115 VAC power, but do not connect any external devices to the unit yet.

On the console rear panel, depress the upper portion of the white power switch. Within about 30 seconds, warm-up should be complete and the appropriate display should appear in the upper left area of the screen. For the basic 3601 terminal this will be in single height characters:

INTECOLOR 3601 CRT MODE V10.80-32E

or similar. (The figures following the V indicate the date of the software, which may be revised from time to time.)

For units with user RAM the display in red, cyan, yellow and green 2X characters will be:

```
DISK BASIC V9.8Ø COPYRIGHT (C)
MAXIMUM RAM AVAILABLE?
15665 BYTES FREE
READY
```

or similar. (A unit with 32K user RAM will show 32Ø49 BYTES FREE)

If the screen display does not appear, pressing the CPU RESET key usually will bring it up unless a serious problem exists.

For a check of the display size, erase page with a background color other than black:

1. If not in the CRT Mode, operate the CPU RESET key.
2. Operate the CAPS LOCK key to the locked down position.

3. Operate the BG ON/FLG ON key.
4. With the CONTROL key held operated, operate a color key, such as RED (the Q key). Release the CONTROL key.

5. Operate the ERASE PAGE key.

The raster in the selected color should be approximately 7.25 x 9.5 inches. The blinking white cursor is visible at the upper left corner of the raster.

To verify convergence, use a full-screen display of white letters against a black background:

1. With the CONTROL key held down, operate the black (P) key.
2. Operate the FG ON/FLG OFF key.

3. With the CONTROL key held down, operate the white (W) key.
4. Select double height characters by operating the A7 ON key.

5. In sequence, operate the (ESC), (TEST)Y and L keys.

There should be a full-screen display of double-height L characters, in white against a black background. Over the entire display the red, blue and green colors should be superimposed on one another reasonably well to yield white letters. (The 36ØØ Series Intecolor unit was in alignment when shipped from the factory. After shipment, in some cases touch-up of the convergence adjustments in the older delta gun units may be necessary and sometimes degaussing may be required. These procedures are described in Section IV of this manual.)

Operate the CPU RESET key. The screen display should be:

```
CRT MODE V9.8Ø
```

or similar.

To test transmit and receive via the RS-232-C serial I/O port, operate in sequence the (ESC) and F keys. This sets the full duplex terminal mode. The screen should display the appropriate characters when the alpha keys are operated. Operate the (ESC) and H keys in sequence to enter the half duplex mode. Now when an alpha key is operated the screen will display the character twice -- once as a result of the key operation and again as a result of the transmit-receive loop. Remove the wire jumper from the MODEM socket. Operate the (ESC) and F keys in sequence. Now when alpha keys are operated, the screen will not display the characters — they are sent only to the RS-232-C output port. Operate the CPU RESET key to regain control.

If the unit has user RAM, operate the (ESC) and the W keys in sequence. The screen display should be:

```
DISK BASIC V9.8Ø COPYRIGHT (C)
MAXIMUM RAM AVAILABLE?
```

Operation of the RETURN key will bring the response:

```
15665 BYTES FREE
READY
```

(or, for a 32K unit, 32049 BYTES FREE)

If the unit has an internal disk drive, open the door of the disk drive and insert the sampler diskette in the drive (label to the right when the diskette is inserted in a 5.25" Mini-Disk drive). Close the door of the disk drive unit. Operate the AUTO key. The diskette "Menu" should appear on the screen within a few seconds. Follow the menu instruction to use one of the programs on the diskette. (Note that either the SHIFT or the CAPS LOCK key must be in the down position when giving an ALL command via the keyboard.) The resulting displays should appear normal. To terminate operation of the program, operate the "↓" cursor down key or CPU RESET. Remove the diskette from the disk drive.

Removal of the diskette from the drive after use is good practice. Occasionally damage to the recorded program occurs at power turn-on or turn-off if the diskette is in the drive unit.

Operate CPU RESET to return to the CRT mode. Turn power off by depressing the lower portion of the power switch. The unit is now ready for connection of external devices.

Peripheral Devices

When connecting external devices to the console, power should be off in both the console and the external device.

To connect the external disk drive to the 3650 Series unit, connect the edge connector of the drive's flat flexible cable to the EXT DISK board area at the left rear of the console, dark colored stripe to the left as viewed from the console rear. (Standard configurations have no more than one external disk drive unit — single or dual. However, additional drives may be added through multiples off this same connection.)

Connect the disk drive unit's power cord to a source of AC power (standard is 60 Hz, 115 VAC, 3-wire). Operate the console power switch on and then the power switch of the external disk drive. The drive is ready for test with the sampler diskette.

The external micro-disk drive of the 3621 Intecolor is connected as follows. With power off the 3621 unit, locate the keyboard edge connector at the rear of the console -- the edge connector at the extreme left on the Logic Module. Note that the color stripe on the flexible cable is to the left, as viewed from the console rear. Gently remove this connector from the Logic Module edge. Connect the external disk drive cable to the Logic Module J1 in its place, color stripe to the left. (The even numbered terminals of the connector are uppermost.) Then connect the keyboard's edge connector to the branch on the cable of the external disk drive, color stripe to the left as before. The system is now ready for use with the external micro-disk drive.

If connection to a modem or other device is to be made, the user provides the necessary cabling and any required interface device.

For an RS-232-C compatible modem, the terminals on the 25-pin connector at the console rear are shown in the table below. The usual modem connections are indicated; however, the modem manufacturer's instructions should be consulted.

Modem Term. No.	Signal
1	AA - Protective Ground
2	BA - Transmitted Data
3	BB - Received Data
4	CA - Request to Send
5	CB - Clear to Send
7	AB - Signal Ground
20	CD - Data Terminal Ready

The length of the cable between the Intecolor and the device connected to the RS-232-C output should not exceed 50 feet.

If the unit is to be connected directly to a host computer (directly, rather than through modems or some other interfacing device), it probably will be necessary to interchange the "transmit" and "receive" leads in the cabling. (The host computer's receive will be the Intecolor's transmit and the host computer's transmit will be sending to the Intecolor's receive.)

Certain serial-type printers may be operated from the RS-232-C serial I/O port. Again, in some cases it may be necessary to interchange the "transmit" and "receive" leads for operation. For some types of printers the baud rate can be important for good operation. Standard Intecolor units default to 9600 baud with one stop bit. (Special configurations may default to a different baud rate.)

To change the baud rate:

1. Operate CPU RESET to enter the CRT Mode.
2. Operate A7 ON if one stop bit is desired. For two stop bits, operate BL/A7 OFF.
3. Operate the (ESC) key, then the R key.
4. Operate a number key to specify a baud rate -- see table below.

BAUD RATE SELECTION

Number Key	1	2	3	4	5	6	7
Baud Rate	110	150	300	1200	2400	4800	9600

The 50-pin bus at the rear edge of the Digital board (to the right, as viewed from the console rear) allows considerable flexibility for connection of user-designed devices.

It provides access to the system data bus, to the address bus, to DC power and several other signals -- see schematic drawing.

In the 3601 and 3621, DC power drain from the +5V supply should not exceed one ampere; the -5V drain should not exceed 250 milliamperes and the +12V drain should not exceed 500 milliamperes. The load on other lines should not exceed one TTL load per line.

The cable to the interfacing device should be kept short -- leads over 6 inches in length may cause problems.

In the 3650 Series units, drain on the power leads should be minimal -- they are intended primarily for sensing. The buffered lines of the X-Bus can support more than one TTL load, but the unbuffered lines should not be loaded in excess of that amount.

Initial Alignment

The 3600 Series Intecolor unit should be in alignment when received from the factory. For the older units with the delta gun CRT, in some cases touch-up of the convergence adjustments on the recessed front panel may be necessary. Degaussing sometimes is required. The procedures are outlined in Section IV.

Installation of the Compucolor II

Installation and initial test of the Compucolor II is very much the same as that described for the 3600 Series units except for the difference in the port connectors. The Compucolor II uses edge connectors at the rear edge of the Logic Module, visible through an opening at the rear of the console near the bottom of the cabinet, for both the keyboard and the serial I/O port.

The keyboard edge connector is mated to the J1 area of the Logic board. J1 is nearest the side of the console. Terminal 2 of the connector is uppermost. Connect the keyboard before initial power-up of the unit. If the unit has an external disk drive, the keyboard and disk drive are multipled off the same J1 area of the Logic board.

The power cable plugs into a socket at the rear of the console. The power switch is adjacent to the socket.

Verify correct operation of the keyboard/console combination before connecting any peripheral devices.

At power-up the unit normally initializes in BASIC. The number of bytes shown as free depends upon the amount of user RAM. Operation of the CPU RESET key initializes the unit in the terminal mode.

Tests may be made as outlined for the 3600 Series units earlier in this section. However, if a test in full duplex is desired, use of an edge connector with terminals 3 and 5 shorted is recommended. The shorting connector goes on the Logic board J2 area near the keyboard connector.

For use with a modem, the usual connections are listed below. However, the modem manufacturer's instructions should be consulted.

Logic Board J2 Term. No.	Modem Term. No.	Signal
1	1	AA - Protective Ground
3	2	BA - Transmitted Data
5	3	BB - Received Data
7	4	CA - Request to Send
9	5	CB - Clear to Send
14	7	AB - Signal Ground
15	20	CD - Data Terminal Ready

The serial I/O port (J2) alternately can be used with a serial type printer. However, the Compucolor II software does not include printer drivers.

The Compucolor II includes the 50-terminal edge area on the Logic board as described in Appendix D of this manual.

SECTION IV

ADJUSTMENT AND ALIGNMENT

IV. ADJUSTMENT AND ALIGNMENT

Section Content

This section describes the adjustment and alignment procedures for the Intecolor 3600-Series Terminals.

All Intecolor units are completely adjusted and thoroughly tested before shipment from the factory. In normal use, no more than minor touch-up adjustment should be required. Product current in 1984 uses pre-converged in-line cathode ray tubes, so the convergence adjustments associated with delta gun CRTs are not required. Units of older manufacture which use the delta gun CRT may require convergence touch-up and/or degaussing from time to time. Following repairs, all adjustments should be checked while the unit is in the shop.

Important! Please read the entire applicable procedure before beginning adjustment. The job goes more smoothly when you know how to obtain a stable display of approximately the correct size at power up.

Preliminary

Hazards — First, a few words regarding possible hazards:

WARNING! Any maintenance performed with power on and cover off subjects the operator to electrical shock hazards that could cause injury or death. Such maintenance should be performed only by trained and qualified service personnel who are aware of the existing hazards.

WARNING! Operate the unit on single phase AC power only. The power supply protection circuit is designed for single phase only. Do not attempt to operate 220-volt units on standard U.S. domestic two-phase 230 VAC.

WARNING! The upper line voltage limit (250 VAC) must not be exceeded — the line filter, fuse, fuseholder and switch are rated at 250 VAC maximum.

Temperature: In all cases, the temperature of the unit should be fairly stable when final adjustments are made. For initial adjustments, if the unit has been stored under unusually cold or warm conditions its temperature should be in the operating range (+10° to +40° C) for at least 30 minutes before proceeding.

Power Voltage: **Verify that the AC power to be used is correct for the unit involved.** All standard units manufactured by the Intecolor Corporation are intended for use with single phase AC power only.

The standard 3600-Series unit uses 115 volts 60 Hz. Options provide for operation at 220 volts 50 Hz. In no case shall the upper voltage limit of 250 VAC be exceeded.

Touch-Up vs. Complete Alignment: The instructions in this section assume beginning the procedure after repair of the Analog Assembly or after substantial misadjustment has occurred. For routine touch-up adjustment of an operating unit, some steps may be omitted.

Tools and Instrumentation

Adjustments are more easily made when the correct tools and instruments are available. Tools include:

#2 Phillips screwdriver (for cabinet screws and one adjustment).

10" screwdriver with flat blade 1/8" or slightly less, shaft insulated. (The blade should be similar to that of a jeweler's screwdriver, for adjustment of small potentiometers. Commonly available plastic tools also may be used.)

3-32" hex plastic alignment tool (for inductors in newer units).

5/16" hex socket wrench or screwdriver with 1/4" flat blade (for removal of analog unit when required for repair).

Instrumentation needs include:

Multirange voltmeter, digital recommended

40KV high voltage probe or meter

Test oscilloscope, DC to 15 MHz

0-1 DC milliammeter, insulated for at least 35KV, with connectors for insertion into the CRT anode path (This meter is recommended for adjustment of the CRT beam current. An alternate procedure is given for use when this meter is not available.)

Enclosure Removal

Power should always be off when the console's enclosure is being removed.

Use a Phillips type screwdriver to loosen the two screws securing the top cover. In a unit with the detached keyboard, the screws are near the front on either side of the cover. In a chassis which includes the keyboard, the screws are recessed under the front edge of the keyboard.

Lift the front of the cover several inches to allow the cover to be slid forward out of its rear retaining groove. Then lift off. (NOTE: On older units, disconnect the fan cable from the analog.)

Section Plan

The procedure for terminals and microcomputers manufactured in 1984 is given first. Procedures for units of older manufacture follow.

3600-Series with In-line CRT
Adjustment Procedure

First, please read pages 4.01 and 4.02 of this section, noting the warnings and the preliminary cautions. Then note the following:

WARNING! Never apply power to the unit with circuit boards improperly secured or resting haphazardly on metal frame parts or on the inner surfaces of the cabinet. Short circuits and/or dangerous voltages on the frame could result. (The inside surfaces of the base pan and cover are coated with a conductive paint.)

Configuration Check

The analog board in the 3600-Series unit with the in-line CRT has been used in other units. The use determines cerain components and jumper positions. If there is any question as to the configuration, it may be checked as follows.

Jumpers are in positions W1 and W4 (NOT W2 or W3).
Q11 normally is present and the Q12 is empty.
C69A is 4700 pF.
R94 is 1K.

For other components, please see Table 1 on the schematic drawing 102350.

The above configuration assumes operation at 60 Hz power frequency. For operation at 50 Hz, Q12 may be used rather than Q11.

Fusing and Line Voltage

Verify that the voltage selector switch SW2 on the Analog board is in the correct position for the power voltage to be used — 115V or 220V. SW2 is in the rear corner of the analog, near the power switch.

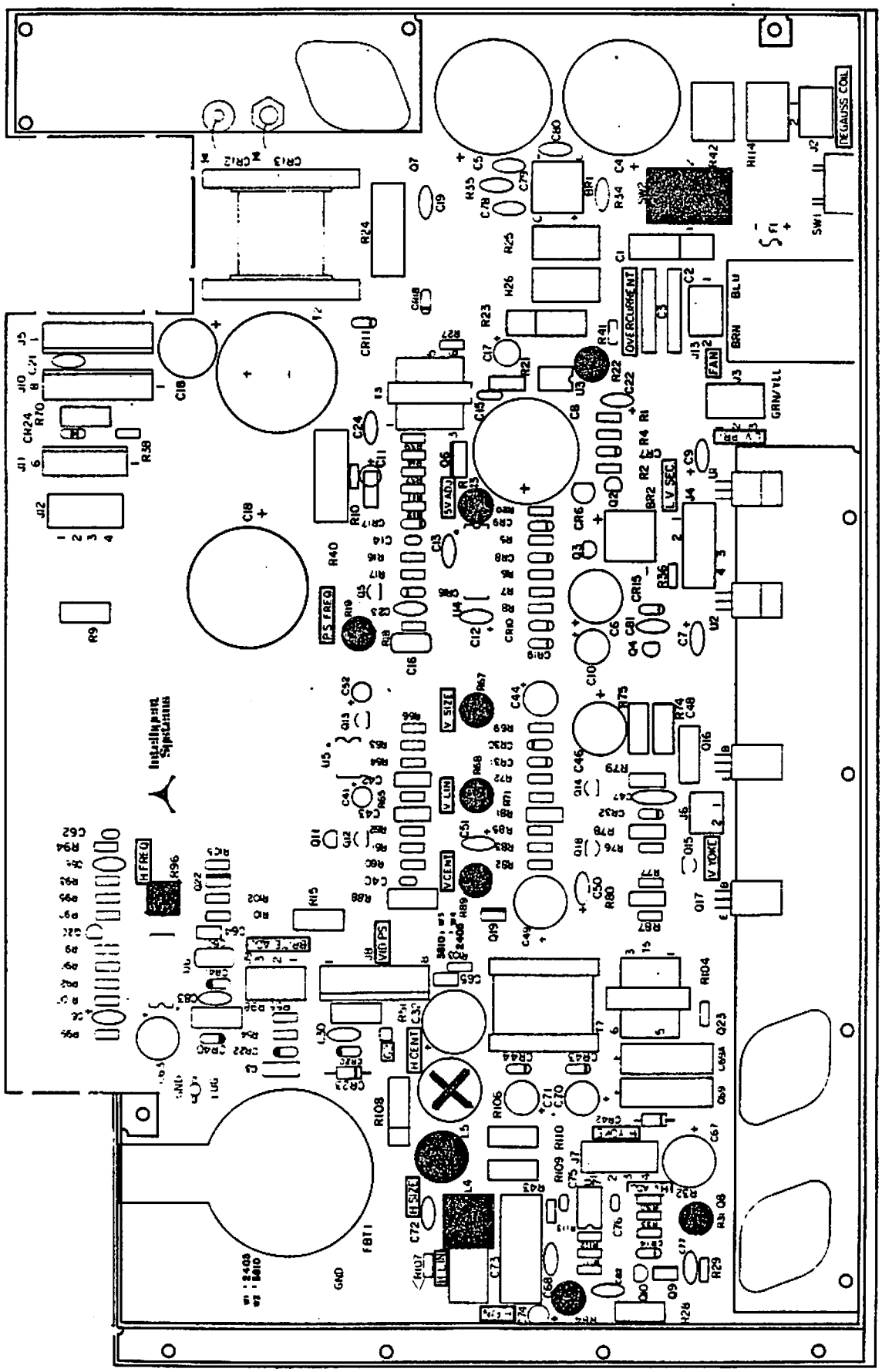
Verify that the line fuse is correct for the voltage to be used:

1.5A, 250V "Slo-Blo" for 115V operation
0.75A, 250V "Slo-Blo" for 220V operation

Complete Adjustment vs. Touch-up

For routine touch-up adjustments of a normally operating unit, all connections may remain intact and the various controls may be left as-is initially. The procedure can begin with the +5V adjustment, page 4.06.

The locations of the controls are shown on page 4.04. If there is a question as to the position of the controls, they may be preset as listed on page 4.05.



Analog -- 3600 with In-line CRT

If substantial maladjustment of the controls is suspected, they may be pre-set as follows.

Analog Board

R13	+5V Adj.	Mid-range
R19	Pwr. Sup. Freq.	Mid-range
R22	Overcurrent Sens.	** As-is

(** Leave the overcurrent adjustment as-is unless suitable loads are available for use in adjustment.)

R31	High Voltage Adj.	Mid-range
---	Focus	Mid-range
---	Screen CRT G2	**As-is
R115	Brightness	3/4 CW

(** The CRT G2 control is on the left side as viewed from the rear. The lower ceramic shaft, the shorter one, usually sealed, is G2. Leave it as-is if the seal is intact. Turn it fully CCW if the seal has been broken. The longer ceramic shaft is FOCUS. The BRIGHTNESS control is on the rear panel.)

R96	Hor. Freq. (Hold)	3/4 CW
R106	Hor. Centering	Mid-range
L4	Hor. Linearity	Arbitrary
L5	Hor. Size	Slug in
R67	Vert. Height	Mid-range
R68	Vert. Linearity	Mid-range
R89	Vert. Centering	Mid-range
R84	Pincushion	Fully CCW

Video Board

Video Gain controls R3, R6 and R17	3/4 turn CW

Following repair, or where substantial maladjustment is suspected, it may be best to disconnect several components prior to adjustment of the power supply. The disconnections advisable depend upon the type of repair. The following are suggested. Remove the cables from:

Analog J5	(Power to Logic Module)
Analog J6	(Vertical Deflection Coil)
Analog J7	(Horizontal Deflection Coil and HV Interlock)
Analog J8	(Video Board Power)

Usually there is no need to disconnect the degaussing coil (from J2) or the fan (from J13) unless the line fuse is failing and one of these items is suspected to be the cause.

Double-check the position of SW2 — the line voltage selector switch.

Low Voltage Check and Adjustment

Apply power to the unit. Then use a voltmeter, preferably digital, to verify the presence of DC voltages as follows. The reference is chassis ground or Analog J5 terminal 5 or 7.

Analog J5 terminal 8	Approximately +5 VDC Adjust the +5V ADJ R24 to obtain +5.1 VDC
Analog J5 terminal 4	+12 +/- Ø.6 VDC
Analog J5 terminal 6	-12 +/- Ø.6 VDC
Analog R9 "hot" end	+7Ø +/- 9 VDC

The OVERCURRENT R22 ADJUSTMENT normally should not be changed. In case of doubt, it should be fully colckwise (CW).

Following verification of the level of the +5V supply and other regulated supplies, if cables were disconnected earlier, turn power off.

Reconnect all cables at the Analog board.

Verify all connections.

Routine touch-up adjustments begin at this point.

+5V Adjustment

Apply power to the unit. Adjust **Analog** board **R13 (+5V ADJ)** to obtain **exactly +5.1Ø VDC** (+Ø.Ø5V/-Ø.ØØV) at **Analog J5 pin 8**, using J5 pin 7 as the ground reference.

NOTE: The objective is +5.ØV at the Logic Module.

High Voltage Adjustment

Turn power off and allow a minute for capacitors to discharge. Connect the ground lead of a high voltage meter or probe to the 36ØØ metal chassis. Then slip the meter probe under the CRT anode cap. The probe tip must make good metal-to-metal contact with the anode cap connector.

After the high voltage probe has been connected, apply power to the unit.

If necessary, adjust the HOR FREQ ADJ R96 to obtain a stable display. Adjust BRIGHTNESS and FOCUS to obtain a readable display.

Press the ERASE PAGE key to clear the screen to black. Then adjust **Analog** board **R31 (HV ADJ)** to obtain a meter indication of **25KV**.

Next, erase the screen in the background color white.

Press the BG ON key (to enable background color selection).
Press the white color key (or the W key with CONTROL held down).
Press the ERASE PAGE key.

The high voltage should change no more than 1KV as the screen goes from black to white.

Turn power off and disconnect the high voltage meter probe from the unit. Disconnect the meter ground lead last.

X-RADIATION

In a properly adjusted 3600-Series unit with a CRT anode voltage of 25KV, X-radiation will average near 0.05 mRh/hr -- well below the government specified maximum of 0.5 mRh/hr. X-radiation will be below this value of 0.5 for anode voltages up to 32KV. However, we strongly recommend that the anode voltage be set no higher than 25KV.

Horizontal Frequency Adjustment

The free-running frequency of the horizontal oscillator in U6 on the Analog board must be adjusted a bit below the frequency of the horizontal sync from the Logic Module.

Use a DC voltmeter to measure the voltage at U6 pin 9. Adjust **R96** to obtain an indication of **between +6 and +7 VDC.**

Create a full-screen pattern of double-height L characters.

Press the 2X CHAR ON key to select double-height characters.
In sequence, operate the ESC key, the Y key and the L key.

If necessary, readjust R96 to make the L characters as straight as possible, noting especially the upper row of characters.

If R96 is too far either CW or CCW, synchronization with the video from the Logic Module is lost, resulting in a garbage display. If R96 is within the synchronization range but not at the optimum point, the vertical lines in the upper row may be slanted right or left.

Power Supply Frequency Adjustment

The power supply switching frequency also is adjusted to make it a bit lower than that of the synchronized horizontal oscillator. Use an oscilloscope to monitor the signal at the collector of Q2 on the Power Supply board.

Sweep speed of 10 microseconds per division.
Vertical deflection sensitivity of 5V per division.
DC coupling.

With **Analog** board **R19** correctly adjusted, there is a single, sharply defined switching signal at 55.6 microsecond intervals. Adjust R19 CW until this signal changes. Then return R19 CCW to obtain the correct signal. Continue R19 another 30 degrees CCW.

If R19 is too far either CW or CCW, synchronization of the switching rate with the horizontal scan frequency will be lost. If the power supply switching frequency is not synchronized with the horizontal sweep frequency, the display tends to be unstable.

Display Size Adjustment

Erase the display in the background color green.

Press the BG ON key (to enable background color selection).
Press the green color key (or the R key with CONTROL held down).
press the ERASE PAGE key.

On the Analog board:

Adjust VERTICAL HEIGHT control **R67** for a display height of **7.25 inches.**
Adjust VERTICAL CENTERING control **R89** to **center** the display **vertically.**

Adjust HORIZ. SIZE control **L5** for a display width of **9.5 inches.**
Adjust HORIZ. CENTERING control **R106** to **center** the display **horizontally.**

Adjust PINCUSHION control **R84** to make the **sides** of the display **straight.**

NOTE: With R84 fully CCW, the sides of the display will be noticeably concave. As R84 is turned CW, the top and bottom corners will draw in to straighten the sides.

Display Linearity Adjustment

First, select foreground color green and background color black.

Press the FG ON key (to enable foreground color selection).
Press the green color key (or the R key with CONTROL held down).
Press the BG ON key (to enable background color selection).
Press the black color key (or the P key with CONTROL held down).

Create a display of 24 horizontal lines.

Press the 2X CHAR ON key to select double-height characters.

In sequence, operate the ESC key, then the Y key and then the underline key (the key just left of the left cursor control key).

On the Analog board:

Adjust VERTICAL LINEARITY control **R68** for **equal spacing** of the lines.

Next, create a display of vertical dot-dash lines.

In sequence, operate the ESC key, the Y key and then, with SHIFT held down, the 1 key.

On the Analog board:

Adjust HORIZ. LINEARITY control **L4** for **equal spacing** of the lines.

NOTE: An alternate pattern for use in both vertical and horizontal linearity is the full-screen pattern of double-height L characters. Operate the 2X CHAR ON key. Then in sequence operate the ESC key, the Y key and the L key.

If the linearity control adjustments were changed substantially, it would be well to re-check the display size adjustment again.

Color and Beam Curent Adjustment

The adjustments of beam current and color controls are best made with use of a beam current meter. The meter itself is a simple DC one milliampere meter. However, it must be insulated for 35KV from grounded circuitry and it must have suitable high voltage connectors.

The procedure using the beam current meter will be described first. Then an alternate procedure for use without the meter will be outlined.

Procedure with Beam Current Meter

1. Turn unit power off. Allow a minute for capacitors to discharge.

2. Use a screwdriver to break the seal holding the "screen" CRT G2 control -- the shorter of the two white ceramic controls on the Deflection Circuit board. Turn the G2 control fully counter-clockwise.

   NOTE: Do not adjust the G2 control in absence of the beam current meter unless absolutely necessary!

3. Turn all three color controls on the Video Driver board, R3, R6 and R17, fully counter-clockwise. Turn the unit's BRIGHTNESS control fully clockwise.

4. Apply power to the unit. Then erase the screen in the background color black. (Operate BG ON, black color key or CONTROL P, and ERASE PAGE).

5. Turn the G2 control slowly in a clockwise direction until a faint full-screen display is seen.

6. Erase the screen in the background color green. (BG ON, green color key or CONTROL R, ERASE PAGE.)

   While observing the beam current meter, adjust the **GREEN** color control on the Video Driver board (R6) to obtain a meter indication of **120 microamperes.**

7. Erase the screen in blue. (Blue color key or CONTROL T, ERASE PAGE.) Adjust the **BLUE** color control (R3) to obtain a beam current of **100 microamperes.**

8. Erase the screen in red. (Red color key or CONTROL Q, ERASE PAGE.) Adjust the **RED** color control (R17) to obtain a beam current of **110 microamperes.**

9. Erase the screen in white. (White color key or CONTROL W, ERASE PAGE.) Turn the BRIGHTNESS control CCW to obtain a display of half intensity.

   Readjust the RED, GREEN and BLUE controls on the Video Driver board, if necessary, to obtain a white screen.

10. Turn the BRIGHTNESS control fully clockwise. The screen should remain white. Total beam current should be between 300 and 350 microamperes.

11. Turn unit power off and disconnect the beam current meter. Re-connect the anode lead to the CRT.

12. Reapply power to the unit. Adjust BRIGHTNESS to a desired level. Check the color of the display with the background erased in the various colors to determine that the color mix is as desired. (BG ON, followed by the color key and then ERASE PAGE. In the 72-key keyboard, the colors black, red, green, yellow, blue, magenta, cyan and white are selected by CONTROL P, Q, R, S, T, U, V and W respectively.)

13. The final adjustment of the G2 control on the Analog board and of the three video gain controls on the Video Driver board should result in a beam current of 300 to 350 microamperes with the screen erased in white and the BRIGHTNESS control fully clockwise.

    With the screen still erased in white, turning the BRIGHTNESS control counter-clockwise all the way should darken the screen.

    With the screen erased in black, and the BRIGHTNESS control returned to the fully clockwise position, a faint raster should be seen.

14. Using the procedure given for High Voltage Adjustment (page 4.20), check the high voltage. With the screen erased in black the CRT anode voltage should be 25KV. It should change no more than 1KV when the screen is erased in white.

    NOTE: There is some interaction between the CRT HV and the G2 adjustments. If the high voltage were increased at step 14, the beam current should be checked again to verify that it does not exceed 350 microamperes at maximum brightness with the screen erased in white.

Procedure without Beam Current Meter

1. Leave the "screen" G2 control on the Analog board at its factory setting unless a change is positively indicated.

2. Erase the screen in the background color white. (BG ON, white color key or CONTROL W, ERASE PAGE.)

3. Turn the unit's BRIGHTNESS control fully CCW. The screen should go dark. If the screen does not go dark, readjustment of the G2 control is indicated. Use a screwdriver to break the seal on the G2 control and turn the G2 control fully CCW.

   Turn the BRIGHTNESS control fully clockwise. On the Video Driver board, turn the RED, GREEN and BLUE gain controls fully CCW.

   Slowly adjust the G2 control clockwise until a very dim raster appears on the screen.

4. Turn the BRIGHTNESS control to about 3/4 CW.

5. On the Video Driver board, adjust the GREEN gain control to within 15 or 20 degrees of fully CW.

6. Adjust the RED and BLUE gain controls to obtain a white display. At this point the display should be approximately half intensity.

7. Turn the BRIGHTNESS control fully CW. The display should remain white and reach satisfactory brightness. The display should not be distorted — note especially the right edge for indication of bulges.

8. Turn the BRIGHTNESS control fully CCW. The screen should go dark.

When the G2 control is correctly adjusted:

The screen is dark with BRIGHTNESS fully counter-clockwise.

With BRIGHTNESS fully clockwise and the screen erased in black, a dim raster is visible.

Satisfactory, but not excessive, brightness is possible with the BRIGHTNESS control near maximum clockwise.

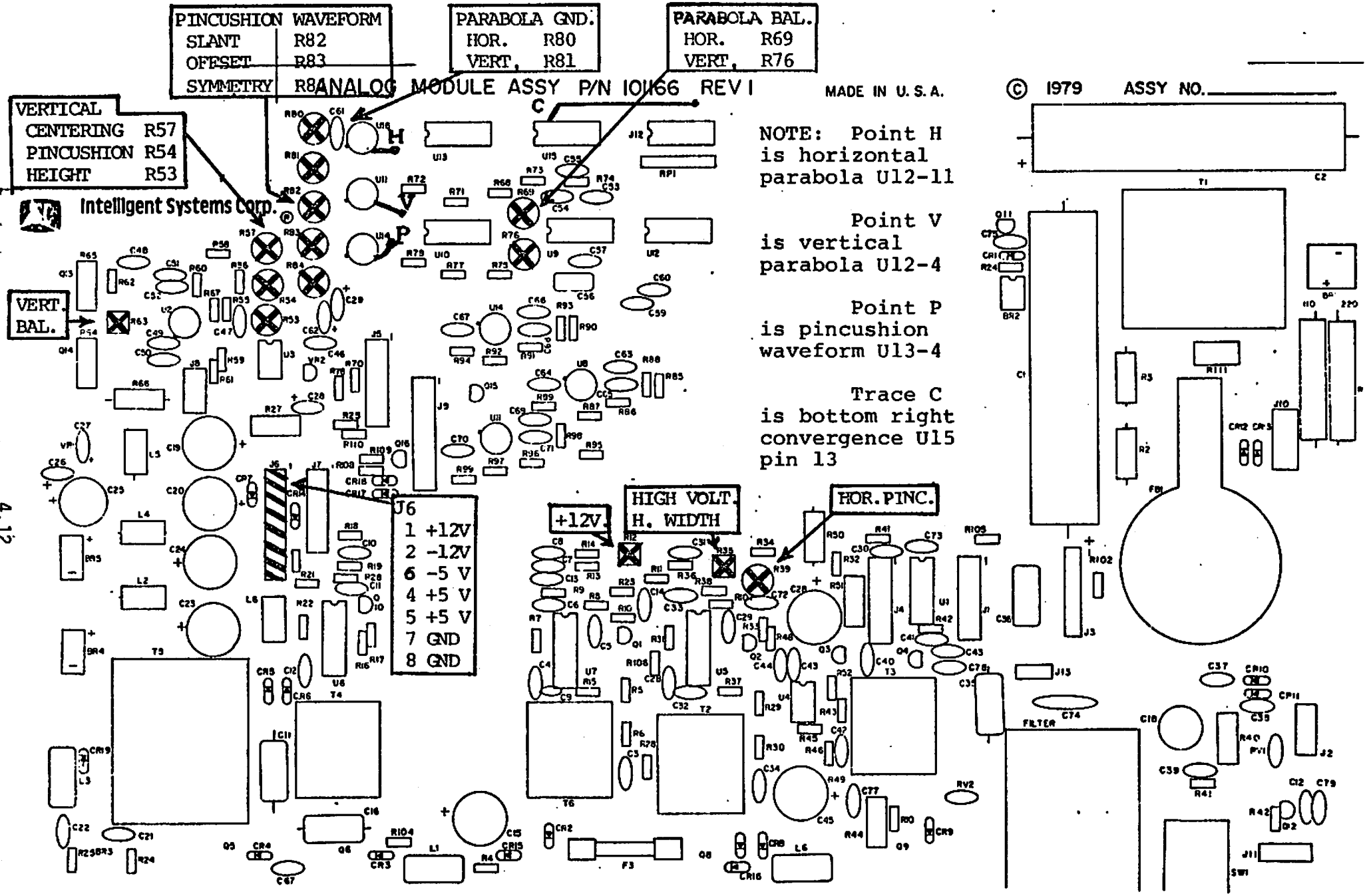
The G2 should be sealed with adhesive to prevent accidental change.

Focus Adjustment

The focus control, the longer of the two white ceramic shafts on the Analog board, is adjusted for best focus over the entire screen. This likely was done automatically during the procedure. It may be checked by placing a full-screen pattern of dots or characters on the screen — e.g., ESC, Y, period.

Adjust the FOCUS control for best focus over the entire screen. The dots should have no trailing edges. (Trailing edges indicate the CRT beam current is too high.)

This completes the adjustment of the 3600-Series unit with the in-line CRT.


PINCUSHION WAVEFORM
SLANT R82
OFFSET R83
SYMMETRY R8
PARABOLA GND.
HOR. R80
VERT. R81
PARABOLA BAL.
HOR. R69
VERT. R76
ANALOG MODULE ASSY P/N 10166 REV I
MADE IN U.S.A.
© 1979
ASSY NO.
VERTICAL
CENTERING R57
PINCUSHION R54
HEIGHT R53
Intelligent Systems Corp.
VERT. BAL.
NOTE: Point H is horizontal parabola U12-11
Point V is vertical parabola U12-4
Point P is pincushion waveform U13-4
Trace C is bottom right convergence U15 pin 13
J6
1 +12V
2 -12V
6 -5 V
4 +5 V
5 +5 V
7 GND
8 GND
+12V
HIGH VOLT.
H. WIDTH
HOR. PINC.
FILTER

4.12

Older Delta Gun CRT 3600 Units
Alignment Procedure

Preliminary

First, note the warnings and cautions on pages 4.01 and 4.02 before proceeding.

Alignment procedures should be performed at the normally available line voltage, preferably 115 VAC for the standard unit (or 230 VAC, if that option is in effect).

For simple touch-up of convergence, see the paragraphs on "Dynamic Convergence" later in this section. This procedure requires only snap-out of the Convergence module cover (front panel, lower right of CRT, small plate with ISC logo) and a small screwdriver for adjustment of the potentiometers. The recommended order of adjustment should be followed.

For complete alignment, before applying power remove the console's molded cover. Remove the two screws recessed in the extreme front edge of the cover. Carefully lift up the front edge of the cover and tilt back. The cover will slip forward out of its retaining groove in the rear framework. Control potentiometer positions should be approximately correct as the unit is received from the factory. If there is any possibility that these have been changed, verify that the HORIZONTAL WIDTH-HIGH VOLTAGE control (R35) is no higher than mid-range. (See Analog Module Assembly Drawing 101166 for location of controls.) Following corrective maintenance or suspicion of tampering, it may be well to begin by presetting all Analog module controls to the center of the range.

Low Voltage Adjustment

Use a digital voltmeter, or instrument of similar accuracy, to measure the +5V supply at J6 terminal 4 on the Analog board with respect to chassis ground, J6 terminal 8. On the small circuit board mounted vertically at the left end of the Analog Module (as viewed from the rear), adjust R12 (small square white potentiometer near top of board) to obtain exactly +5.0 VDC. Now measure the voltage from J6 pin 1 to ground. On the main Analog board, below the rear of the CRT yoke, adjust another R12 to obtain exactly +12.0 VDC. Other DC low voltages may be checked as follows:

From	To	DC Voltage
Analog J6-6	Ground	-5 + 0.25
Analog J6-2	Ground	-12 + 0.6
Q14-collector	Ground	+23 + 10%
Q13-collector	Ground	-23 + 10%
Video J1-3	Ground	+40 + 10%
R16-R17 Junction	Ground	+27 + 10%
U10-14	Ground	+12 + 0.6

NOTE: Older 3601 or 3621 units have only one adjustment for both +5 and +12 VDC. R12 on the main Analog board is adjusted to obtain both +5 + 0.25 and +12 + 0.6 VDC, with the +5 "favored".

The +300 VDC unregulated supply is not referenced to chassis ground. Any instrumentation connected to circuits associated with this supply must be isolated from ground. Connect the ungrounded instrument's common lead to the negative terminal of C2 (the large blue capacitor at the right side of the Analog PCB, as viewed from the rear. The positive lead of the instrument may be touched to F2 (fuse holder mounted on rear panel, identified as "H.V.") to measure the +300V (+300 + 10%).

High Voltage Adjustment

With power off, connect the ground lead of a high voltage meter (capable of measurements to 35KV) to the chassis and the probe to the anode connector on the CRT.

> **CAUTION!** Be sure the ground lead of the HV probe is connected to frame ground and that the HV probe itself is isolated from equipment other than the CRT anode and anode lead — and also is isolated from personnel.

Apply power and allow a couple of minutes for warm-up. Erase the display with the background color red and verify (by the appearance of the rectangular raster) that both vertical and horizontal sweep circuits are operating. On the Analog board, adjust the HORIZONTAL WIDTH-HIGH VOLTAGE control R35 to obtain a display width of 9.5 inches. The high voltage should be between 22KV and 25KV.

X-RADIATION

The specifications for CR Tubes list the maximum allowable X-radiation as 0.5 mR/hr. For all ISC systems in current production X-radiation typically is below 0.05 mR/hr. at 25 KV. The maximum allowable anode voltage for the delta gun 13" CRT is 27.5 KV. Even at this maximum anode voltage the X-radiation is less than 0.5 mR/hr.

Degaussing

With the terminal oriented north-south (or in place in its normal viewing location), degauss the unit by moving a degaussing coil (such as a GC 9317) in a circular pattern over the face of the CRT and around the sides of the unit. While continuing the circular pattern in the same direction, gradually withdraw from the front of the unit to a distance of six feet or more before disconnecting the coil from its AC power source.

Vertical and Horizontal Deflection

With the display erased with the background color red, on the Analog board adjust the VERTICAL HEIGHT control R53 and the VERTICAL POSITION control R57 to obtain a display height of 7.25 inches centered vertically. The horizontal width was adjusted to 9.5 inches by use of R35 under High Voltage Adjustment (described above). In the 3650 Series units, the horizontal centering was factory-adjusted. (If a change is necessary, the jumper field at the right rear of the Logic Module is used. See sheet 2 of drawing 101354, lower left quadrant, for jumpers W5, W6, W9 and W10.)

In the 3621 and older 3601 units, center the display horizontally by adjustment of R20 on the Digital board. (R20 is a small potentiometer readily accessible at the rear edge of the board, just left of the keyboard connector.) Note that when R20 is adjusted the pattern moves in discrete two-character jumps. Adjust the pot by touch to leave it half-way between jump points. (The pattern may tear if the adjustment is too close to a jump point. A full-page pattern of the letter Z makes a good test for satisfactory adjustment.)

Pincushion Adjustment

With the screen still erased in the background color red, observe that the top and bottom of the raster are straight horizontal lines. Adjust the VERTICAL PINCUSHION control R54, if necessary, to obtain this condition.

Adjust the HORIZONTAL PINCUSHION control R39, if necessary, to obtain straight vertical lines at the left and right edges of the raster.

Vertical R54

Horizontal R39

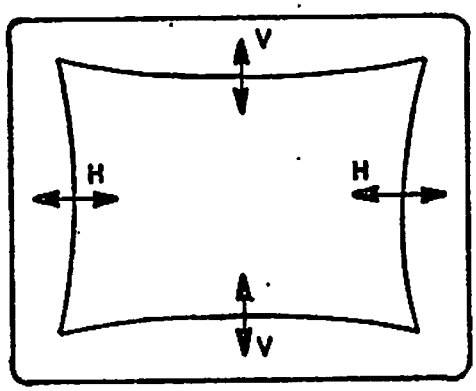


Figure 4.01

Static Convergence

Place a single white letter (such as a double-height L) at the center of the screen, background black. Adjust the FOCUS control R101 (mounted on the right of the rear panel, the upper control) for optimum focus. Verify that all potentiometers on the Convergence module (under snap-off cover, lower right of CRT front) are centered (straight right position).

Now adjust the static magnets and the blue lateral magnet to align the red, green and blue colors of the center screen letter so the letter appears white. This occurs when the red, green and blue colors are accurately superimposed on each other. The beams move at approximately the same angle as the convergence magnets are offset from the vertical. Blue, since it is mounted in the vertical plane, moves the beam up and down; red and green move the respective beams on a line at about 60° from the vertical. The blue lateral magnet moves all three beams in the horizontal plane, the blue beam in one direction and the red and green beams in the opposite direction in a 5 to 1 ratio. The blue beam has the greatest lateral shift. (The thumb screw adjustments of the red, green and blue center convergence magnets can be rotated in either direction continuously. Flux change is accomplished by rotating the pole position of the magnets, not by moving the magnets farther from or closer to the respective guns.)

Purity

Before proceeding with purity adjustment, first verify that the center of the raster is properly converged, as described in the preceding paragraph. (Note: The unit should be in either its normal viewing position or oriented in a north-south position during purity adjustment.)

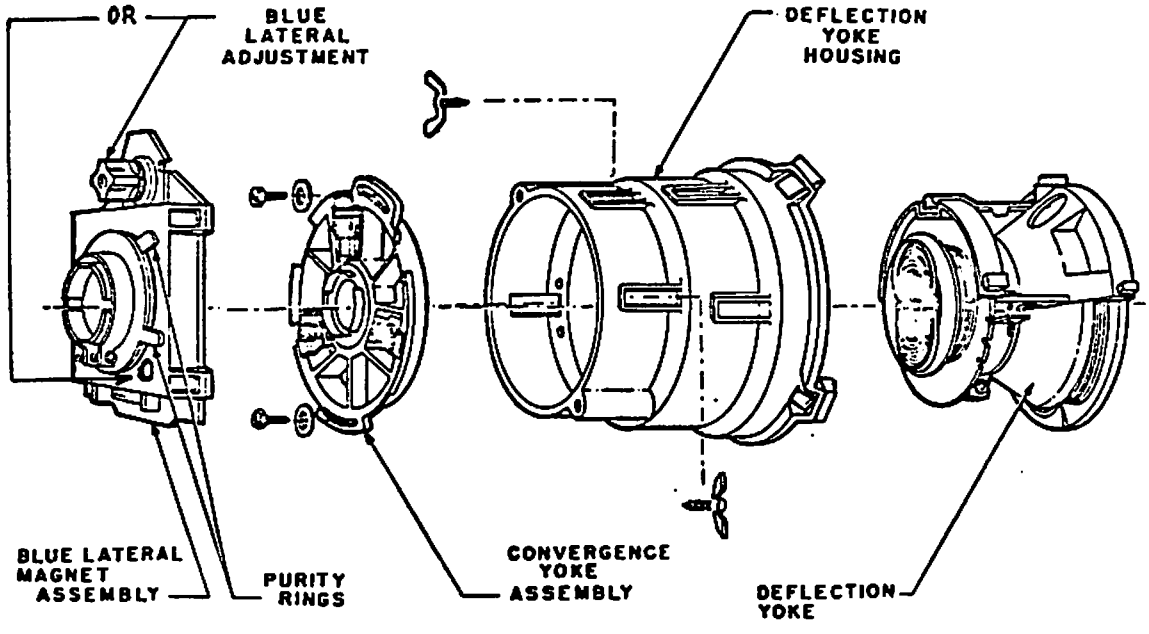
1. Erase the screen with the background color red.

2. Loosen the yoke wing nuts and move the yoke to the rear as far as possible (see Figure 4.Ø2).

3. Rotate the purity magnets (rings) and adjustment tabs to obtain a clean red area at the center of the screen. Then push the yoke forward until a uniform red raster is obtained. Tighten the yoke wing nuts.

4. Touch up the VERTICAL HEIGHT and HORIZONTAL WIDTH controls if necessary to obtain the correct display size (7.25 x 9.5 inches). (There should have been very little change. However, if the horizontal width was increased very much in this readjustment, it would be well to re-check the high voltage to be sure it is not excessive.)

5. Readjust static convergence (p. 4.15) if required. (The Purity and Static Convergence adjustments have some interaction.)



YOKE ASSEMBLY
Figure 4.Ø2

Color Temperature Adjustment

1. Erase the screen with the background color white.

2. Turn the screen grid controls on the Video Module — R2 (RED), R1 (BLUE) and R3 (GREEN) — fully CCW. Turn the BRIGHTNESS control R113 (mounted on the rear panel, below the FOCUS control) to maximum brightness (fully CW).

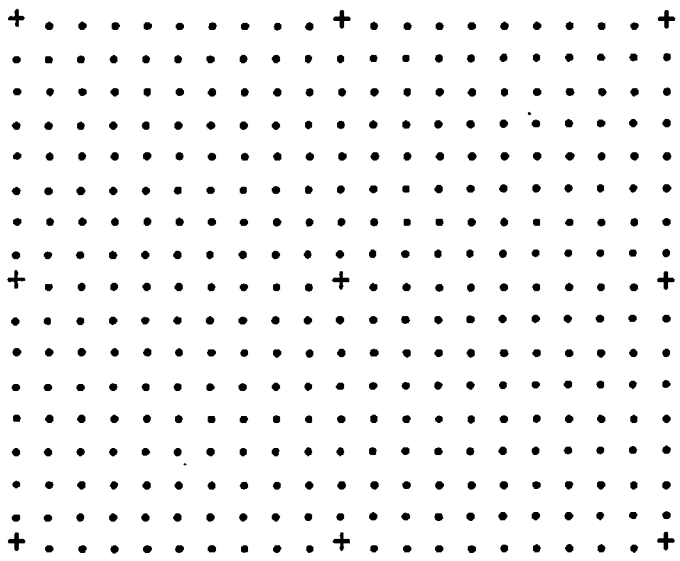
3. Turn the RED control R2 clockwise until the red vertical raster line at the top of the screen is just visible. Repeat a similar process for the GREEN control R3 and the BLUE control R1.

4. Adjust the BRIGHTNESS control R113 until there is no visible vertical retrace raster line and the brightness is at a comfortable viewing level with a minimum of color saturation.

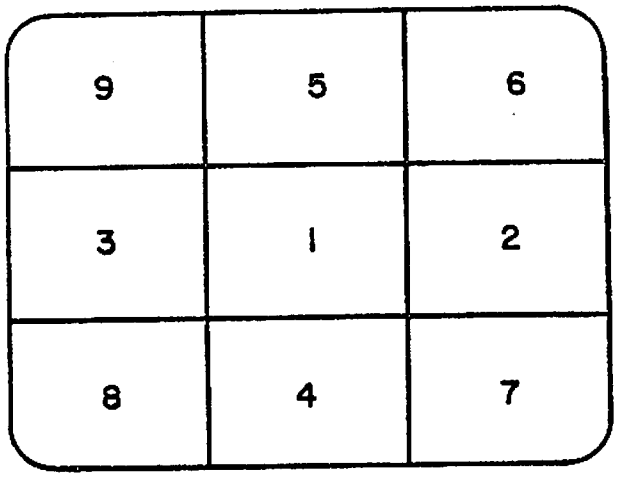
5. Touch up the adjustment of these controls as required to obtain a white screen at a comfortable viewing level of brightness.

Dynamic Convergence

Place a pattern of white dots on the screen, background black. Place + symbols or letters such as L or H at the corners, screen center and midway along each side, top and bottom (see Figure 4.Ø3; or use a full-screen pattern of the letter "L", obtained by operating the ESC, Y and L keys in succession). Touch up the FOCUS adjustment for optimum focus over the entire screen.

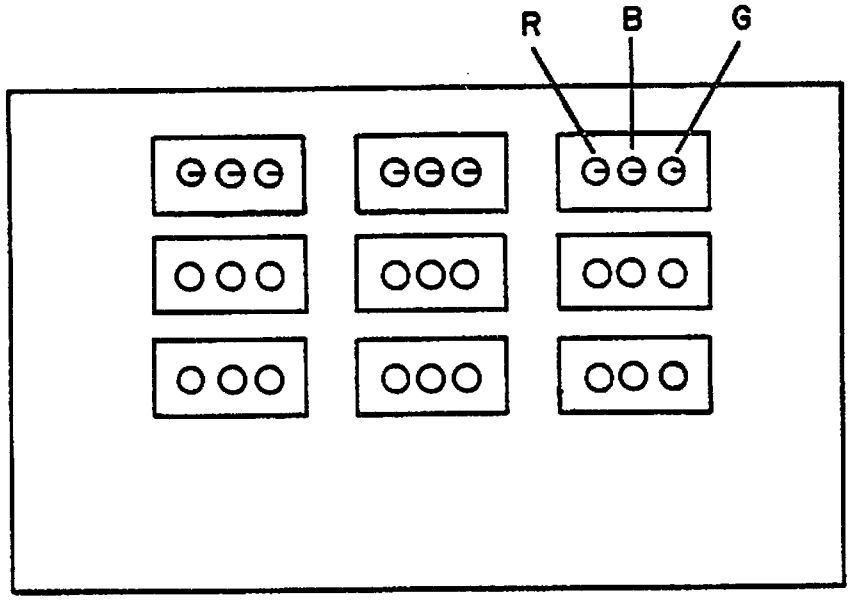


CONVERGENCE PATTERN
Figure 4.Ø3



CR Tube Convergence Sectors (Screen View)

Figure 4.Ø4



Convergence Module

Figure 4.Ø5

Begin with all controls on the Convergence Module at or near center position (straight right). Then touch up the center convergence -- which should already be fairly good if the static convergence was done with care -- by adjustment of the center group of pots on the Convergence Module (RED R5, GREEN R3, BLUE R4). See Figures 4.04 and 4.05.

Once center convergence has been adjusted, make the convergence adjustments for screen sector 2 (see Figure 4.04). Then proceed with convergence adjustments for other sectors in numerical order. After each sector is converged, check and touch up the center convergence. (Note that the adjustment pots on the Convergence Module are arranged in the same location as each screen sector, screen viewed from the front. In each of the sector pot groups there is one pot for each of the three colors.)

After adjusting all nine sectors as described above, touch up each screen sector as needed in the SAME ORDER. Do not violate the order of the screen sector numbers in the adjustment procedure.

Never attempt a convergence procedure without first setting the Convergence Module pots to the center position and then following the order of the screen sector numbers.

If satisfactory convergence cannot be obtained by the procedure outlined in the preceding paragraphs, check the following adjustments in the Analog Module.

Convergence Circuit Adjustments

Readjustments of convergence circuit controls R69, R76 and R80 through R84 are necessary only when problems in convergence (as described in preceding paragraphs) are encountered, when corrective maintenance has been performed in this circuit area or when tampering with the adjustments has occurred. The procedure requires the use of an oscilloscope (Tektronix T922 or similar) to view the waveforms in the Analog Module.

The following instructions identify waveform locations which are readily found on the schematic. However, these points are not always the most accessible on the chassis. The board layout on page 4.12 identifies four points more easily reached: Point H for the horizontal parabola, Point V for the vertical parabola, Point P for the pincushion waveform and Point C for the bottom left corner convergence waveform. The left, right, top and bottom convergence waveforms also are accessible at the terminals of potentiometer chips on the Convergence Module -- pin 2 of the center left, center right, top center and bottom center potentiometer chips respectively. The corner convergence waveform is available on the right-hand of two vertical conducting paths between the bottom left and bottom center potentiometer chips.

1. Horizontal Ramp and Preliminary Parabola Adjustments are made while observing the horizontal parabola at U12-11 (or Point H). Adjust R69 to make the parabola end points equal in height (see Figure 4.06).

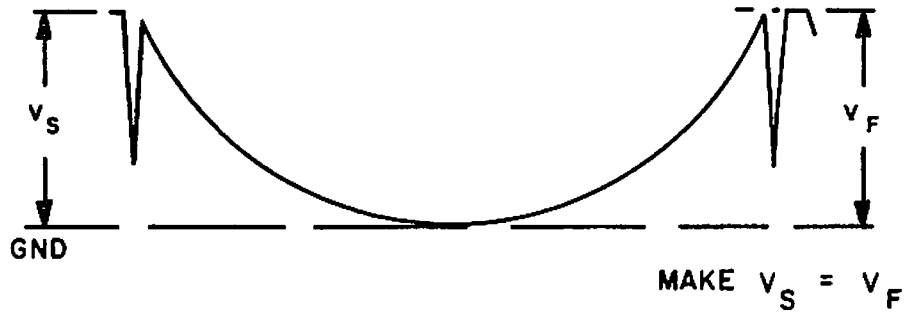


Figure 4.06

Adjust R80 to place the bottom of the parabola at ground level (see Figure 4.07). This adjustment affects convergence in the right center and left center screen areas.

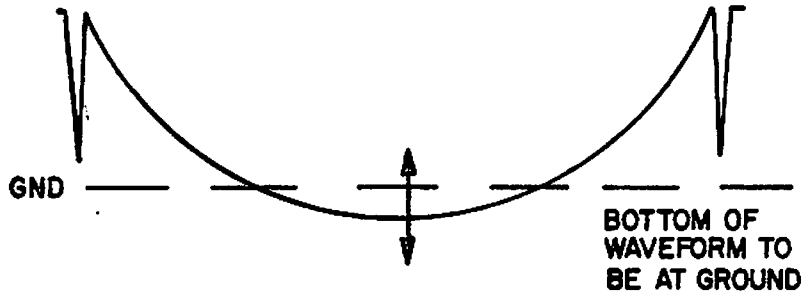


Figure 4.07

2. Vertical Ramp and Preliminary Parabola Adjustments are made while observing the vertical parabola at U12-4 (or Point V). (The pattern is similar to that shown in Figures 4.06 and 4.07 except for the difference in time and the absence of pronounced "dips" between successive parabolas.) Adjust R76 to make the parabola end points equal in height. Adjust R81 to set the bottom of the parabola at ground level. This adjustment affects convergence in the top center and bottom center screen areas.

3. Corner Parabola Adjustments (affecting convergence in the four corner areas of the screen) are made while viewing the pincushion waveform at U13-4 (or Point P).

OFFSET is adjusted to zero by using R83 to bring the waveform baseline to ground level (see Figure 4.08A).

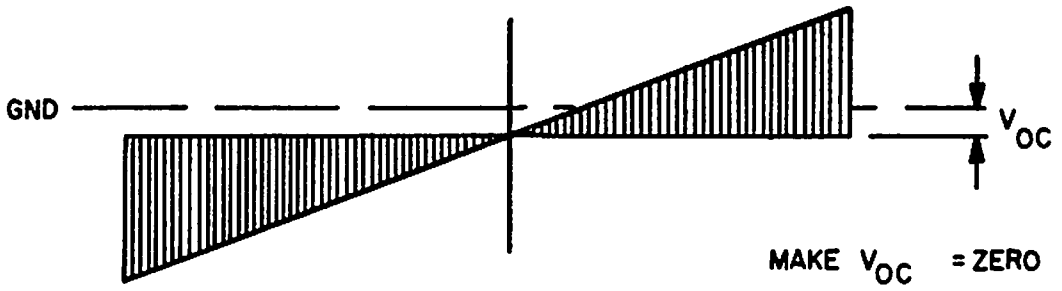


Figure 4.08A

BASELINE SLANT is adjusted by using R82 to make the waveform baseline horizontal (see Figure 4.08B).

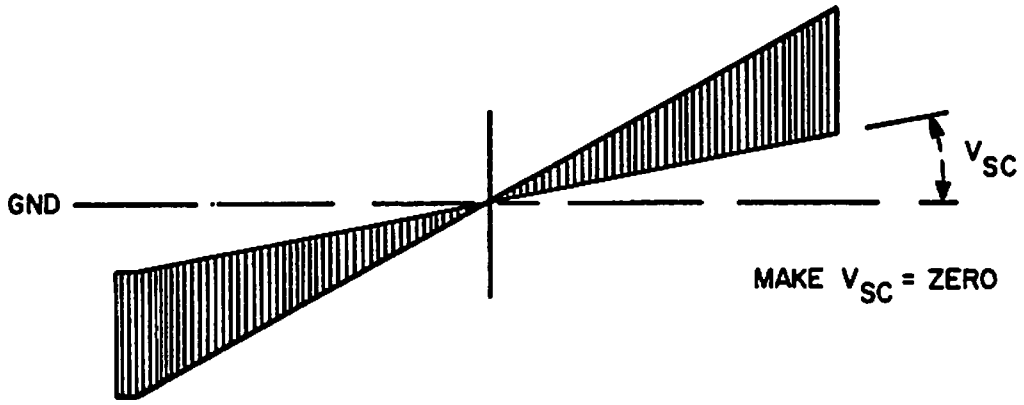


Figure 4.08B

VERTICAL SYMMETRY is adjusted by using R84 to make the heights of the waveform triangles equal (see Figure 4.08C).

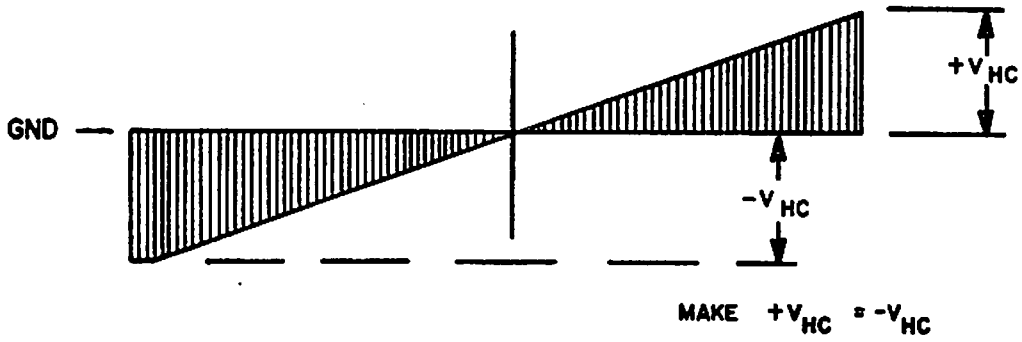
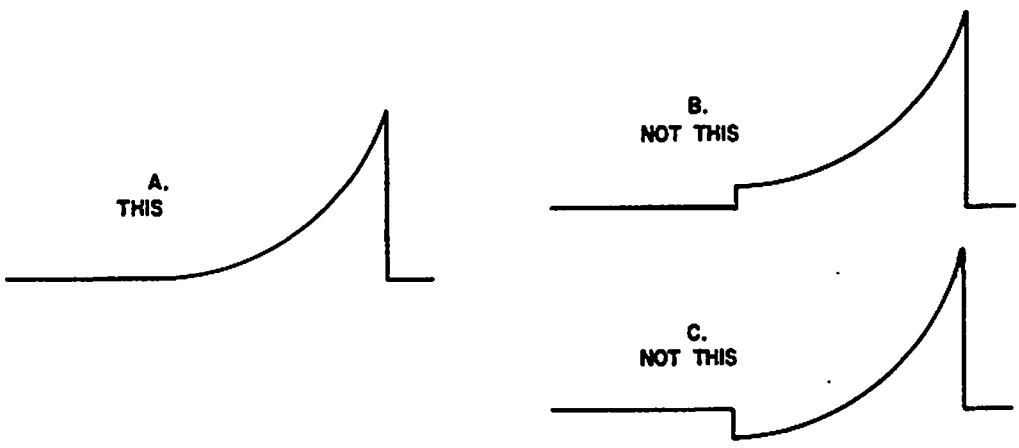


Figure 4.08C

4. Horizontal and Vertical Parabola Final Adjustments can best be accomplished by monitoring the waveforms being sent to the Convergence Module.

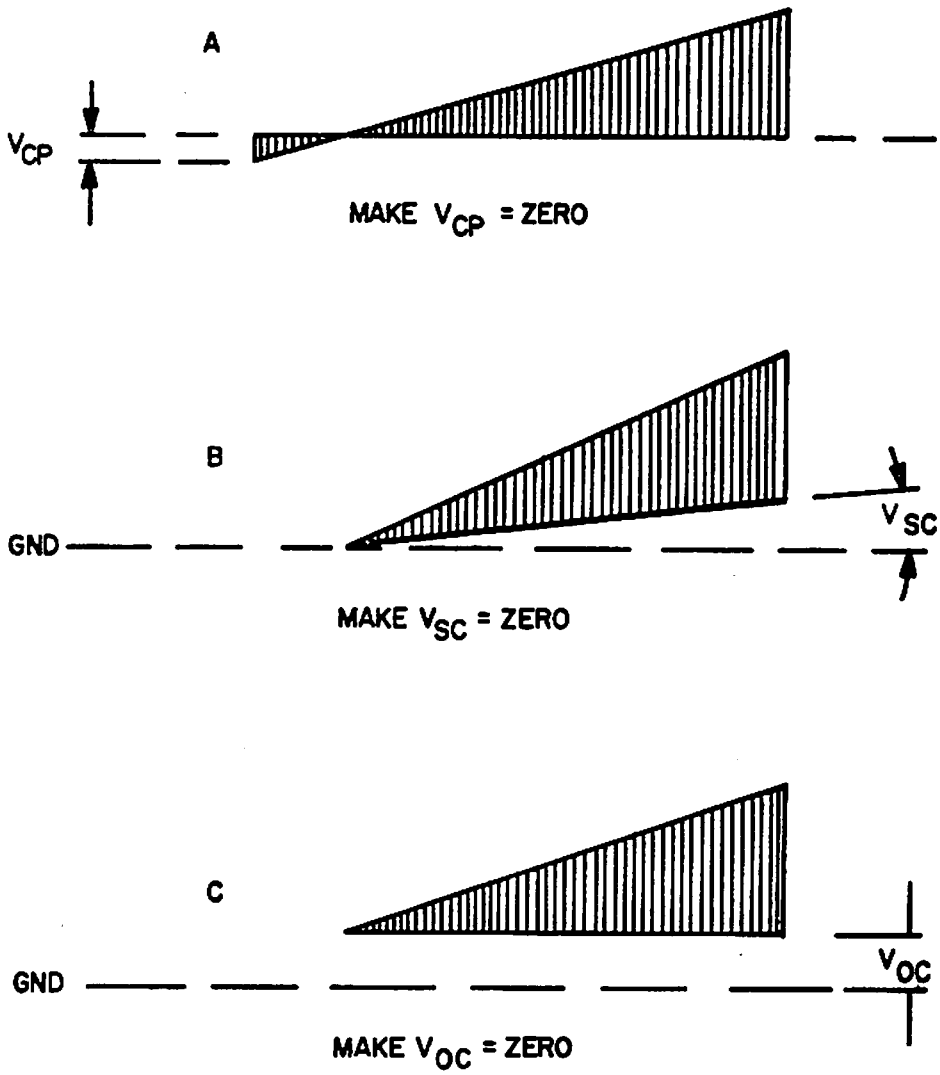
While observing the waveform at terminal 2 of the right center potentiometer chip on the Convergence Module, adjust Analog R80 to make the horizontal offset zero (see Figures 4.09A, B and C).



Figures 4.09 A, B, C

Observe the waveform at terminal 2 of the bottom center potentiometer chip and adjust R81 to make the vertical parabola offset zero in similar fashion.

5. Corner Parabola Final Adjustments are made while observing the waveform at U15-13 or, preferably, at the conducting path running between the bottom left and bottom center potentiometer chips on the Convergence Module — the right-hand of the two paths. Adjust R84, R82 and R83 to obtain a single triangular pattern with baseline horizontal and no base offset from ground. (See Figures 4.10 A, B and C.)



Figures 4.10 A, B, C

Whenever these convergence circuit controls on the Analog Module are readjusted, follow immediately with the Dynamic Convergence adjustment procedure described earlier in this section.

Vertical Output Balance Adjustment

The adjustment of the Vertical Output Balance control R63 should be checked whenever parts such as U2, Q13 or Q14 in the Analog Module are replaced or whenever there is evidence of Q13 and/orQ14 overheating.

1. Adjust VERTICAL HEIGHT R53 and VERTICAL PINCUSHION R54 to zero (fully CCW).

2. Use an oscilloscope to measure the voltage at the junction of R64-R65 (with respect to ground). Adjust VERTICAL POSITION R57 to obtain zero voltage.

3. Measure the voltage at the junction of R66 and J8-1 (again with respect to ground). Adjust VERTICAL HEIGHT R53 to obtain a ramp height of +1.8 volts (3.6 volts peak-to-peak).

4. With the oscilloscope isolated from AC ground and chassis ground, connect the common lead of the oscilloscope to the end of R64 connected to the Q14-emitter (the end toward the rear of the chassis). Connect the probe to the end of R65 connected to the Q13-emitter (toward the front of the console). Adjust VERTICAL OUTPUT BALANCE R63 to bring the tip of the triangular waveform about 25 millivolts below ground level. (Placing the tip a little below ground level insures that both transistors are not off at the same time. Placing it much too far below ground level causes them to conduct excessively and overheat.)

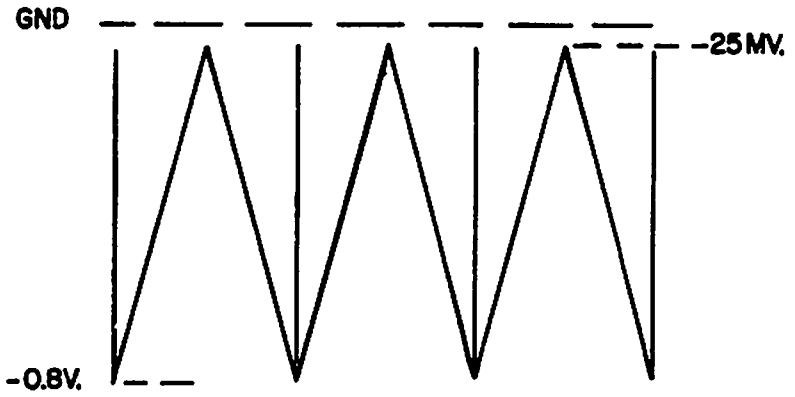


Figure 4.11

5. Disconnect oscilloscope.

6. Erase the screen with the background color red.

7. If necessary, readjust VERTICAL HEIGHT R53 and VERTICAL POSITION R57 to obtain a display 7.25 inches high and centered vertically. Adjust VERTICAL PINCUSHION R54 to obtain straight top and bottom edges. (Horizontal width and centering should not have been affected by these adjustments.)

Disk Drive Speed

The Micro-Disk Drive Assembly used in the 3621 Intecolor has a strobe disk on the drive wheel for speed check. For check and adjustment of drive speed, view this strobe under 60 Hz. fluorescent light. With no diskette in the drive, operate the keyboard AUTO key to cause the drive to run. The outer pattern of the strobe disk should appear very nearly stationary. If there is appreciable drift, adjust R10 on the Disk Controller board to "stop" the pattern. Operate the CPU RESET key to stop the disk drive.

If 50 Hz. power is used, perform the check and adjustment under 50 Hz. illumination and observe the inner pattern on the strobe disk.

The disk drives used with the 3650 Series Intecolor units require no field adjustments.

Note regrading Micro-Disk Drive: Data recorded by a Micro-Disk Drive running faster or slower than the correct speed may not be retrievable on a drive running at the correct speed. Usually it is retrievable if the drive used for recovery is "maladjusted" to the speed, fast or slow, at which the data was recorded. In the Micro-Disk Drive, data can be recovered only when the drive speed is very nearly the same as it was when the data was recorded.

COMPUCOLOR II ALIGNMENT

The Compucolor II cabinet must be partially disassembled for most alignment or trouble-shooting. Exercise care to avoid damage to the Logic module and the Video Driver board during removal of the rear cover. And note the following warning.

> **WARNING!** Any maintenance performed with power on and the cover disassembled subjects the operator to electrical shock hazards that could cause injury or death. Such maintenance should be performed only by trained and qualified service personnel who are aware of the existing hazards.

Cabinet Disassembly

1) With power off, disconnect the keyboard and any other connections to the rear edge of the Logic board.

2) Remove four screws (3 top, 1 bottom) that secure the rear cover to the front portion of the cabinet.

3) With cabinet upright on the bench, slide the rear section back slowly to allow the Logic board to disengage gently from its mounting slots in the rear cover. The cable to the Power board (mounted in the rear cover) will allow the cover to be moved far enough for access to the controls on the Analog board (mounted vertically at the side of the cabinet.).

4) Reconnect the keyboard to the J1 area at the rear edge of the Logic board. Apply power and allow several minutes warm-up.

Low Voltage Adjustment

Use an accurate voltmeter to measure the +5V level between the Logic board J6 terminal 4 and frame ground. Adjust Analog R22 to obtain +5.0 VDC. (This is a very important adjustment. If the +5V supply is even half a volt off, peculiar problems can occur.)

Other low voltages may be checked at points on the Analog board as follows. The reference is frame ground.

E23	-5.1 +/- 0.25 VDC
E20	-12.0 +/- 0.6 VDC
E19	+12.0 +/- 0.6 VDC
E16	-48.0 +/- 5.0 VDC

Noise and ripple on these voltages, as viewed with an oscilloscope, should not exceed 3% peak-to-peak.

There is no high voltage adjustment as such. It may be checked later, after horizontal width adjustment, if desired.

Convergence Circuit Adjustments

For complete adjustment following repair, these adjustments may be checked at this time. They normally are not required for touch-up of an operating unit.

1) Set the four potentiometers at the top of the Analog board — R94, R95, R96 and R97 -- to the center of their range.

   Note the type of Analog board. Later production units may be identified by presence of three ICs, one above the other, near the top inner edge of the board.

2) Monitor the horizontal parabola with an oscilloscope — at U17-3 or U5-2 in older units, at UA7 terminal 3 or 4 in later units.

   Equalize the end points heights by adjustment of R102 in older units, R112 in later units.

   Set the bottom of the parabola at ground level by adjsutment of R101 in older units, R110 in later units. Final touch-up can be made while viewing the half parabola — at U5-1 in older units, at UA7 terminal 2 in later units.

   (For waveform sketches, see pages 4.20 and 4.22.)

3) Adjust the vertical parabola in similar fashion. The waveform may be viewed at U11-3 or U5-9 in older units, at UA7 terminals 11 or 12 in later units.

   Equalize end point heights — adjust R103 in older units, R113 in later units.

   Set the parabola ground level -- adjust R104 in older units, R111 in later units. View the half parabola at U5-8 in older units, at UA7 terminal 13 in later units.

4) The pincushion waveform is not adjustable. However, it should be checked for conformance with sketches on pages 4.21 and 4.22. View the waveform at U16-3 in older units, at UA10 terminal 3 in later units. Ground level, tilt or slant, and triangular symmetry should be within one volt of ideal.

Display Size and Focus Adjustment

1) Erase the screen in the background color red.

   Operate the BG ON key.
   With CONTROL held down, operate the Q key.
   Operate the ERASE PAGE key.

2) Set the pattern height at 6.25" by adjustment of R106. Center the pattern vertically by adjustment of R105 in older units, R129 in later units.

3) Set the horizontal width to 9.375" by adjustment of T109.

Horizontal centering is adjusted by R20 on the Logic board, near the rear edge by the keyboard cable. The pattern will move in discrete two-character jumps. Set R20 by feel midway between jump points.

R20 may be adjusted more accurately by use of a full screen pattern of Z characters.

Operate the BG ON key.
With CONTROL held down, oerate the P key.
In sequence, operate the ESC key, the Y key and the Z key.

4) Adjust the focus potentiometer, on the rear edge of the Analog board, for best focus over the entire screen.

High Voltage Check

Although not adjustable apart from the horizontal width adjustment, high voltage may be checked at this time if the unit is in the shop for repair. With power off, connect the ground lead of a high voltage meter or probe to the Analog frame. Then slip the probe into contact with the high voltage connection at the CRT anode. With power back on, the high voltage should be within the range of 16KV to 22KV.

Purity Adjustment

1) Again erase the screen in the background color red. The red should be fairly uniform over the entire screen.

2) If necessary, rotate the purity rings by their tabs to obtain color uniformity. The rings are on the magnet assembly just to the rear of the CRT yoke.

3) If there is difficulty in obtaining a fairly uniform color, degaussing likely is required. With the degaussing coil held perpendicular to the CRT face, energize the coil. Begin moving the coil in a circular pattern as it is brought parallel to the CRT face and rather close to it. While continuing the circular movement of the coil, move it around the top, sides and bottom of the unit, then back parallel with the CRT face. Continuing the circular movement of the coil parallel to the CRT face, withdraw it gradually to a distance of five or six feet. Then turn the coil perpendicular to the CRT face and de-energize it.

4) In the case of a new CRT, it may be best to move the yoke toward the rear of the CRT neck. Loosen the yoke clamp to slip it back. Then adjust the purity rings to place the red spot at screen center. Move the yoke back forward to obtain a uniform red display a bit more than 6 by 9 inches in size. Note that the pattern has not been rotated as the yoke clamp is tightened.

Pincushion Adjustment

The top and bottom edges of the red display should be fairly straight. Adjust R108 on the Analog board to make the sides of the display as straight as possible. (Note: If the adjustment appears to have no effect, the optical isolator is usually at fault — U4 in the older units, UA2 in the later units.)

Color Temperature Adjustment

1) Erase the screen in the background color white.

   Operate the BG ON key.
   With CONTROL held down, operate the W key.
   Operate the ERASE PAGE key.

2) On the Video Driver board (mounted on the CRT base), turn the three G2 controls fully counter-clockwise — R1, R2 and R3.

3) Turn the red control R1 clockwise until red retrace lines are visible. Then return R1 CCW until the retrace lines and any color outside the normal display area just disappears.

4) Adjust the green control R2 and blue control R3 in similar fashion.

5) The above adjustments may be touched up to yield the desired degree of whiteness at the desired viewing level of brightness.

Convergence Adjustment

1) Create a full screen pattern of white double height L characters or of dots against a black background.

   Operate the BG ON key.
   With CONTROL held down, operate the P key.
   Operate the FG ON key.
   With CONTROL held down, operate the W key.
   Operate the 2X CHAR (or A7 ON) key.
   In sequence, operate the ESC key, the Y key and the L key (or dot).

2) Characters at screen center should appear white if Focus and Purity adjustments were made correctly.

3) On the Analog board, adjust TOP R96 for best convergence at the top of the screen.

4) Adjust BOTTOM R97, RIGHT R95 and LEFT R94 for best convergence in the bottom, right and left areas respectively.

5) Observing the same order of adjustment, re-touch the adjustments of R96, R97, R95 and R94 for best over-all convergence.

Note Regarding Display Shape

In some cases, a "keystone" effect may be observed -- one side of the display, usually the left side, is noticeably greater in height than the other side. This usually can be corrected by what might be considered misadjustment of the horizontal parabola.

With the screen erased in red, readjust R1Ø2 (older units) or R112 (later units) a bit to make the two sides more nearly equal in height. But don't overdo it.

If this correction is required, convergence adjustments must be made again.

Disk Drive Speed

Please see page 4.25 for disk drive speed adjustment.

Cabinet Reassembly

1) With power off, disconnect the keyboard cable from the Logic board. Then verify that all other cables are fully mated and that the Video Driver board is firmly in place on the base of the CRT.

2) Verify that the Logic board front edge is in place in the mounting slots.

3) Bring the rear cover close to its mating position with the front portion of the console.

   The problem in fully mating the rear cover with the rest of the cabinet lies in positioning the Logic rear edge tabs in the slots in the rear cover. Usually this is easier if the entire cabinet is tilted forward to the point where the front portion will maintain its position at an angle. Then the Logic board is more readily visible. The fingers or a small screwdriver or similar can be used to adjust the Logic board position so the tabs fit the rear cover slots as the rear cover is pressed into place.

   Replace the four screws that secure the rear cover to the rest of the cabinet.

4) Reconnect the keyboard cable to the Logic board J1 edge area.

SECTION V

CIRCUIT DESCRIPTION

V. CIRCUIT DESCRIPTION

Overview

The 3600 Series Intecolor unit consists of a molded cabinet housing the following major assemblies:

Assembly	Function
13" Color CRT & Yoke	Eight-color display
Analog Module	System power voltages Sweep and convergence waveforms Line frequency sync
Convergence Module	Convergence adjustment
Video Driver Module	Video signal amplification CRT connections Color mix
Digital Module	Microcomputer Display generator Sync signals for system Serial video signals Disk drive interface (3650 Series)
Keyboard	Manual data input and control
Disk Drive Unit (3651/2)	Data storage and retrieval

The rear edge of the Digital Module, accessible from the console rear without removal of housing, will accept edge connectors for peripheral equipment and there is a 25-pin connector for RS-232-C compatible interface. The upper terminals of the edge connectors have the even numbers.

J1	26-pin	Normally used for keyboard connection Also used for external Micro-disk drive in 3621
J2	26-pin	Serial I/O device connection (RS-232C compatible) Normally cabled internally to a 25-pin ISA connector at the rear of the console
J3	50-pin	For future or user-designed interface devices In the 3650 Series units this area is slotted to accept a 26-terminal edge connector for X-Bus

The 3650 Series also may have an edge connector area on another small board (to the left as viewed from the rear) for external disk drives.

The power switch, the line fuse and one of the +300 VDC fuses are located on the rear panel, as are the focus and brightness controls.

The 3652 has an external Mini-Disk Drive and the 3653 and 3654 units have a dual 8" Floppy Disk Drive. These units have a flat flexible cable for connection to the rear of the console. Each has a separate power cord.

Section Plan

The circuit descriptions deal first with the analog module, video board, digital board and disk controller used in the 3621. A modified version of the digital board was used in early 3601 terminals.

The digital circuitry was redesigned for the 3650 series. The circuit description for this board begins on page 5.44. A modified and physically smaller version of this logic board was introduced in the 3601. Notes regarding this board are on page 5.58.

For a period of time the 3650 series used an analog board similar to that described for the 3621. The principal differences are noted at the bottom of this page.

The circuit description for the analog board now used begins on page 5.59.

Cathode Ray Tube and Yoke

Product manufactured in 1984 uses a 13-inch pre-converged in-line CRT. In older product the CRT is a 13-inch (diagonal measure) delta gun standard resolution 370AKB22 with 0.024" trio spacing. The yoke, convergence coils and blue lateral magnet assembly are similar to standard TV components.

CAUTION! Use only manufacturer recommended replacements for these components in order to assure minimum X-radiation.

ANALOG MODULE NOTE

During the first several months of manufacture the Analog Module has had a number of changes. The principal change involves the +5 VDC power supply and the low voltage unregulated DC. Early units had +15V as the low voltage unregulated supply; later units have +27V. In earlier units the +5V supply came via power transformer T5 and R12 on the Analog board was used for adjustment; later units use the +27V as a source for +5V, the +27V supply being dropped through a series transistor. This transistor is pulsed under control of an SG3524 IC in much the same fashion as are Q7 and Q8. The control circuitry is on a small printed circuit board which is mounted on the side of the Analog wrap — the left side as viewed from the rear of the console. The +5V adjustment is R12 on this small added board; the R12 on the main Analog board is used solely for adjustment of +12V.

Some early units had the CRT heater supply from a winding on the flyback transformer. Current units have a filament transformer, mounted where the transformer for the +15V supply had been. The transformer for the +27V supply is mounted separately.

The circuit description following covers the earlier Analog Module. However, with the above notes considered, it is applicable to most of the circuitry of the current board.

ANALOG MODULE - Early, Delta Gun

The 101166 Analog Module is used in Intecolor units in the 3000, 8300, 8900 and 9000 series. It supplies the system power voltages, including the CRT high voltage, and develops the line-frequency sync signal. Sync signals from the Digital Module are used to synchronize the switching-type power supplies to certain logic frequencies. The Analog Module receives vertical reset, horizontal reset and horizontal drive signals from the Digital Module and uses them in development of eight convergence waveforms and the horizontal and vertical sweep waveforms.

All of the Analog Module circuitry is contained on a single printed circuit board 10 1/8 x 15 7/8 inches. A formed aluminum frame serves for board stiffening and for heat-sinking the power transistors and rectifiers. Assembly Drawing 101166 shows the layout of components on the PCB.

Schematic Drawing 101177 shows the circuits, which will be described as those for:

Unregulated DC voltages
Line-frequency sync
Regulated DC low voltages
Convergence waveforms
Convergence amplifiers
Vertical deflection
Horizontal deflection
Regulated DC high voltage
Video gates

Unregulated DC voltages

Two unregulated DC voltages, +300 V and +15 V, are developed from input AC power. The AC power at 115 volts (optionally 230 volts), 50 or 60 Hz., is brought in through a line filter (see upper left corner of schematic). The line fuse (1.5 A., slow-blow) and power switch are located on the rear panel of the Analog Module frame, with the line fuse accessible without housing disassembly. Varistor RV1 across the line suppresses voltage spikes. R1 connects one side of the AC line to the C1-C2 junction and the +300V rectifier operates as a voltage doubler, using only the upper two diodes in the BR1 bridge package. C1 and C2 serve as filter and R2-R3 as a bleeder resistor. (In the 230 VAC option the BR1 bridge is eliminated. A diode connects one side of the AC line to C1. C1 itself is changed to have a 350-volt rating and has its lower side connected to the other side of the AC line through R1. The C2 terminals are shorted. 300V thus is supplied by a half-wave rectifier rather than by a voltage doubler.)

NOTE THAT THE 300-VOLT SUPPLY IS NOT REFERENCED DIRECTLY TO CHASSIS GROUND. UNGROUNED INSTRUMENTATION MUST BE USED WHEN DEALING WITH CIRCUITS CONNECTED TO THIS SUPPLY. THE 300-VOLT COMMON IS "HOT" WITH RESPECT TO THE CHASSIS.

The +300 VDC is used in development of both high and low regulated DC voltages. F2 (1/2A., fast-blow) fuses the circuit for high voltage and horizontal sweep. F3 (1/2A., fast-blow) fuses the circuit for low voltages.

T1, a step-down transformer, has its primary connected across the AC line through series resistor R1. Bridge rectifier BR2, connected to the secondary of T1, develops approximately 15 VDC across filter capacitor C28. This +15V supply is referenced to chassis ground. (In the 230 VAC input option, a different transformer -- a DST-5-12 replacing the ST-5-12 -- is used to accept 230 volts input.)

Noise and ripple at the outputs of these unregulated supplies typically is less than 10 volts p-p for the +300V supply and less than 1 volt p-p for the +15V supply.

Line Frequency Sync

Approximately 6.5 VAC at the power line frequency is taken from T1 terminal 8 and connected to transistor Q11 through series resistor R24. Diode CR1 clips the negative peak and the base-emitter junction of Q11 clips the positive peak. The output at Q11-collector is very nearly square-wave and has an amplitude of 4 to 5 volts. Figure 5.01 shows a typical line frequency sync waveform.

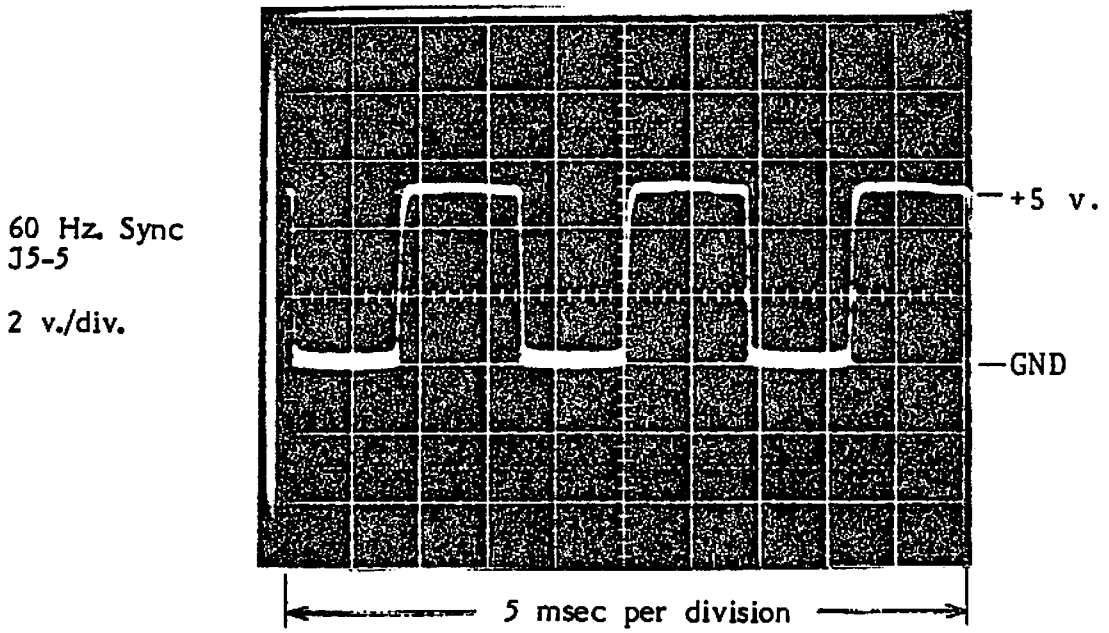


Figure 5.01

Regulated DC Low Voltages

A switching-type power supply generates the regulated low DC voltages used throughout the system. An SG3524 chip U6 (schematic upper center) is used to generate a square wave at the horizontal sweep frequency (near 16 KHz for 32-line units, 24 KHz for 48-line units). This square wave is applied through transformer T4 to drive amplifier transistors Q6 and Q5. The amplifier output through transformer T5 is applied to several rectifiers at a number of voltage levels to obtain DC power. Regulation of the output voltage levels is accomplished by control of the collector voltage to amplifier transistors Q6 and Q5. SG3524 chip U7 and transistor Q7, the IC chip having feedback from the +5V output , control that voltage.

The SG3524, used for both U6 and U7, is an integrated circuit that includes a voltage regulator for reference, an error amplifier, an oscillator, a pulse width modulator, a pulse steering flip-flop, dual alternating output switches and current limiting circuitry. The output switching transistor connections are shown as A and B, with A-collector at pin 12, A-emitter at pin 11, B-collector at pin 13 and B-emitter at pin 14. These output switches are enabled to turn on alternately from zero to not quite 50% duty cycle, depending upon the feedback. An external resistor and capacitor (RT and CT) determine the oscillator period. The oscillator can be synchronized to a somewhat higher external frequency by sync pulses applied at pin 3.

For U6, R22 and C12 set the free-running period to about 70 microseconds. However, an input from the Digital Module through transistor Q10 to pin 3 shortens the period to result in an oscillator frequency of double the display horizontal sweep frequency. For the circuit which determines the output pulse width, U6 obtains a reference voltage from voltage divider R20-R21. The feedback is ground potential at pin 1. The feedback in this case continually indicates "output low" and results in maximum allowable turn-on time for both output switching transistors in U6. The SG3524 is used here as a square wave generator rather than as a voltage regulator. This square wave at the horizontal sweep frequency, with an amplitude of about 5 volts p-p, is applied to the primary of T4.

Figure 5.02 shows the output of Q10 applying sync pulses to U6 pin 3 and the U6 output waveforms. The noticeable spikes in the output waveforms are normal.

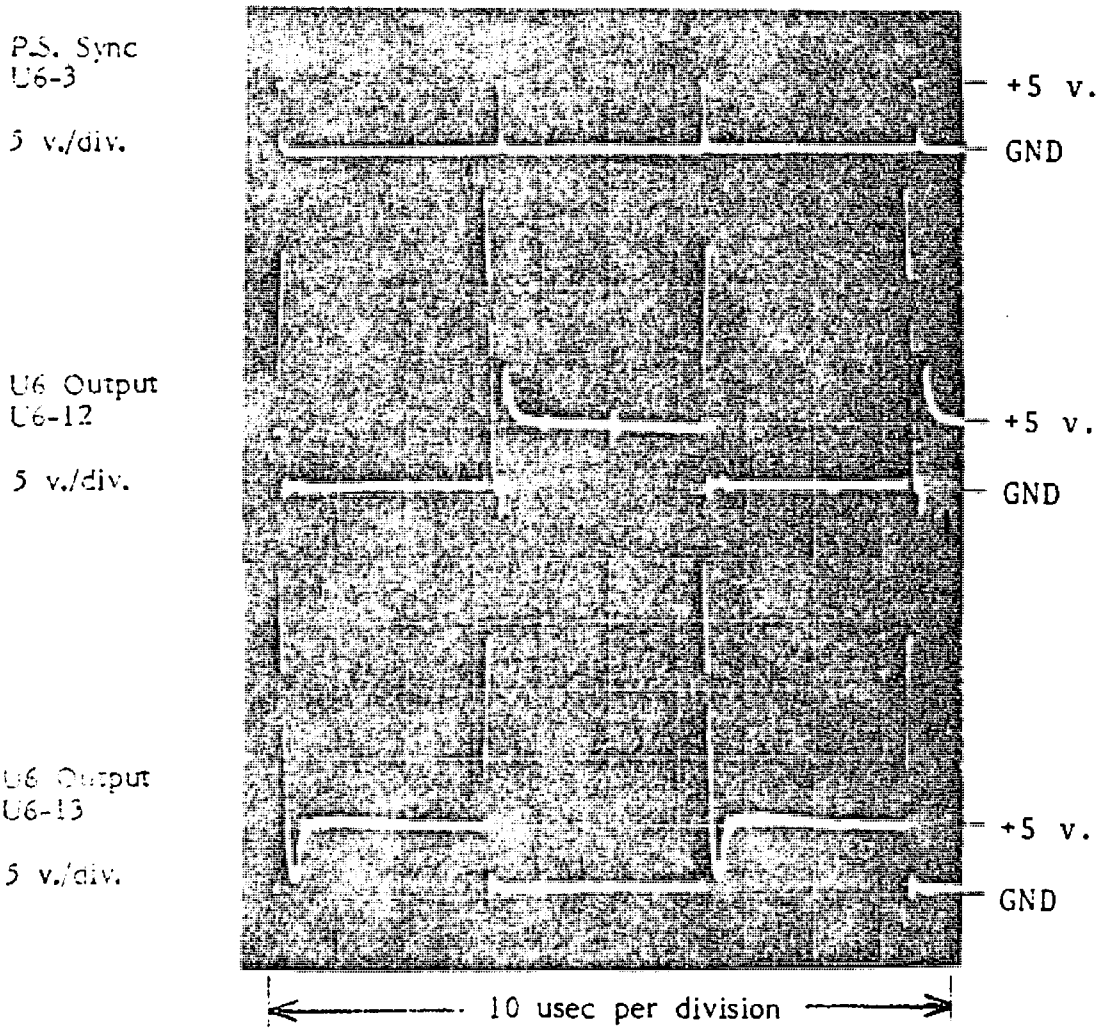


Figure 5.02

At the secondary of T4, this square wave alternately turns on Q6 and Q5. The peak-to-peak voltage of the square wave these power transistors apply to the primary of transformer T5 is very nearly that of the voltage connected to the collector of Q6.

NOTE THAT THE SUPPLY VOLTAGE OF Q6 AND Q5 IS NOT REFERENCED TO CHASSIS GROUND. USE UNGROUNDED INSTRUMENTATION FOR ANY MEASUREMENTS HERE.

Figure 5.03 shows the waveform applied to the primary of T5.

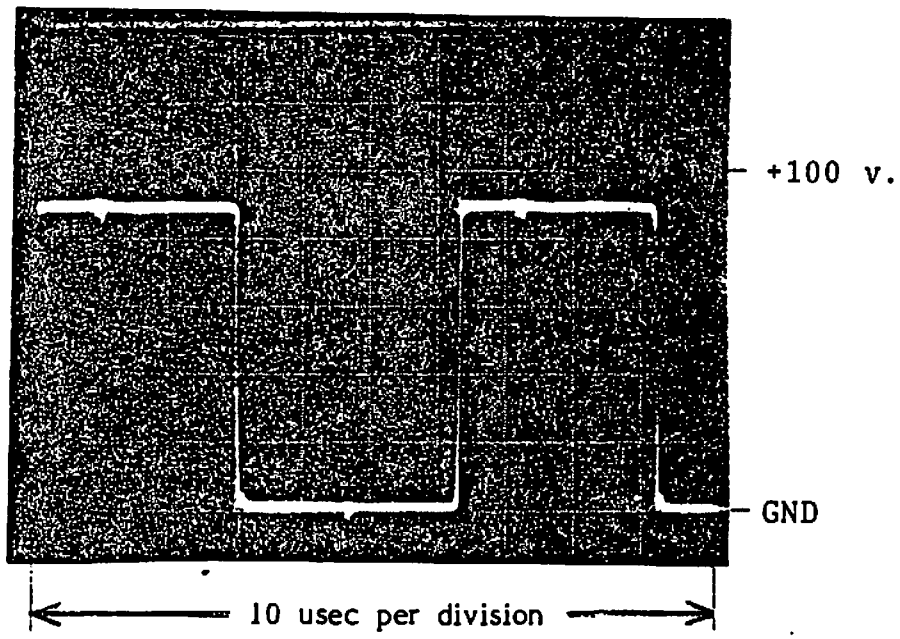


Figure 5.03

The voltage at Q6-c is determined by the duty cycle of transistor Q7, in series with the +300V supply. When the U7 pulse turning on Q7 is wider, the voltage at Q6-c is higher. When Q7 is turned on a lower proportion of the time, the voltage at Q6-c is lower. The width of the Q7 turn-on pulse, applied through T6, is determined by the feedback to terminal 1 of U7.

The SG3524 in U7 varies its output pulse width to function as the voltage regulator. Its output pulse at terminal 12 is at the horizontal sweep frequency, synchronized by the Digital Module through Q1. A reference voltage from voltage divider R8-R9 is connected to U7 pin 2. Feedback from the +5V DC output is connected to U7 pin 1 to control the U7 output pulse width as the load on the supplies changes. The feedback level is adjustable by potentiometer R12 and is adjusted during alignment to set the +5V output to exactly 5.0 volts.

The voltage from Q6-collector to Q5-emitter normally is approximately 100 volts in early production units. The p-p voltage of the square wave across the primary of T5, terminal 11 to terminal 10, has very nearly the same value. In later production a different transformer is used for T5 and the input voltage is nearer 180 volts. In either case the instantaneous value can vary to meet changes in the loads on the +5V.

Figure 5.04 shows the sync pulses at U7 pin 3 and the U7 output at pin 12. The "ringing" seen following each pulse is normal.

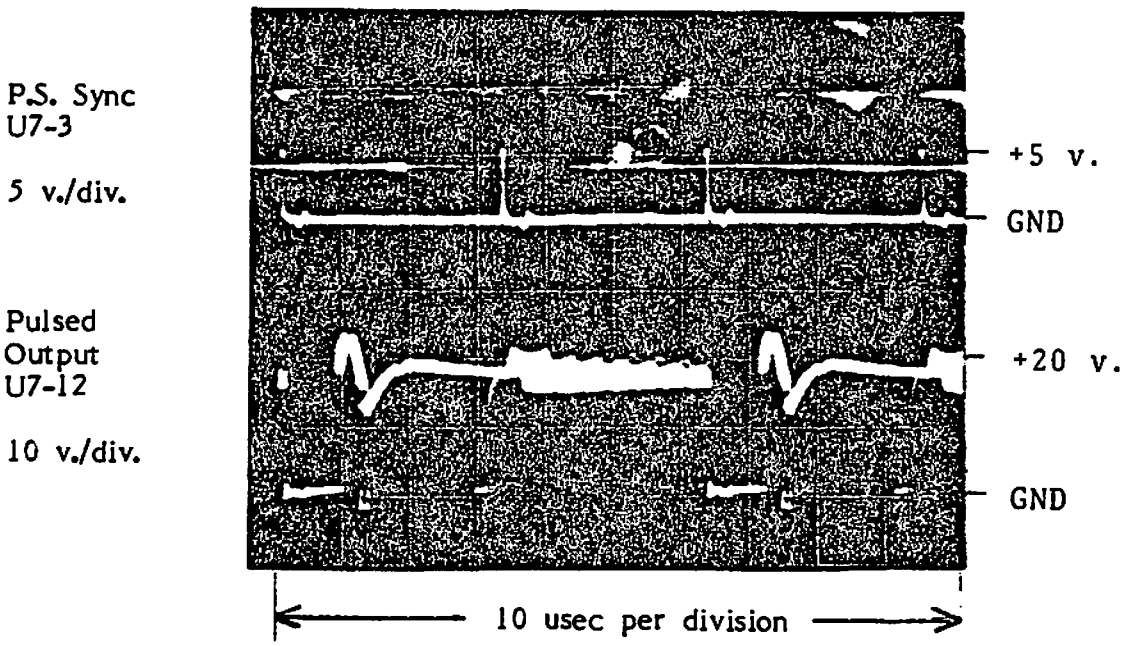
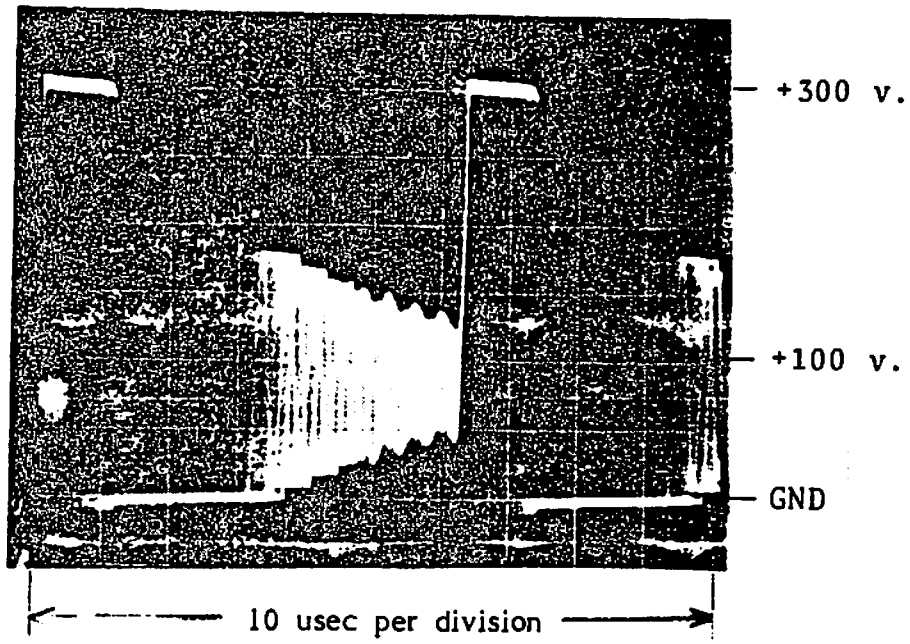


Figure 5.04

Figure 5.05 shows the waveform at the emitter of Q7 (with reference to the 300-volt common, not chassis ground). The very noticeable ringing following each pulse is normal. Here the ringing centers about a level of approximately +100 volts. In later production this center value is nearer +180 volts in accordance with the input requirement of the newer transformer used as T5.

Pulsed
Voltage
Q7-e

50 v./div.



The secondary of T5 has a grounded center tap and several taps for connections to four rectifiers at different voltage levels. For +5V there is a full-wave rectifier BR3 and a filter consisting of L3 and C23. CR19 is used as a protective device to hold the level of the +5V supply to a reasonable value in case of loss of regulation. Normally it draws very little current. The feedback for voltage control is taken directly from the output of rectifier BR3.

For +12V, -15V, -12V, -9V and -5V there is a bridge rectifier BR4. +12V is taken from the positive leg of the bridge. L2 and C24 make up the filter. Feedback for voltage control is taken from the filter output. -15V is obtained directly from the negative leg of BR4. Voltage regulator chip VR1 sets the -12V level, with C27 for filter. -9V is obtained from the -12V supply by dropping the voltage through series zener diode CR7. -5V is obtained by further dropping the level through zener diode CR14.

BR5, with filtering by L5-C19 and L4-C20, supplies +24V and -24V. Full-wave rectifier diodes CR5 and CR6, with filtering by L6-C18, supply +48V. An additional +12V supply for use in the Analog Module only is obtained from VR2 (shown on the schematic just to the left of T5). This regulator has the +24V as input.

All of these low-voltage DC outputs are referenced to chassis ground.

The +5V, -5V, +12V and -12V outputs are used in the Digital Module. (In the 8300 and the 8900 Series the digital boards also use -9V.) The Video Module uses the +48V, -12V and +5V outputs. +24V, -24V, +12V, -12V and +5V are used in other circuits of the Analog Module. The optional Micro-Disk Drives receive their power by way of the Digital Module in the 3600 Series Intecolor. (In the 8300 and 8900 Series units having an internal Mini-Disk or 8" Floppy Disk Drive, a cable from J7 supplies +24V, -15V, +12V and +5V to the drive.)

Convergence Waveforms

Convergence of the three color beams in the CRT is achieved in Intecolor units through nine-sector control. The Convergence Module uses a DC voltage (-12V) and eight waveforms generated in the Analog Module. These eight waveforms are developed in circuitry shown in the lower right portion of the Analog schematic drawing. They are synchronized by pulses from the Digital Module.

A horizontal ramp is developed across capacitor C54 (below a section of U9, near schematic center), the left side of which is connected to a negative voltage through R69 and R68. The horizontal reset pulse from the Digital Module, input through R71, causes one section of U10 to operate and close a switch across C54 to discharge it. This brings the voltage at U9 pin 14 to approximately -6 or -7 volts. When the horizontal reset pulse has passed, the switch "contact" between U10 pins 11 and 13 opens. C54 charges through a section of U9, which serves as a constant current generator (or consider the section of U9 as an operational amplifier with capacity in the feedback circuit to become an integrator). The voltage at U9 pin 14 increases linearly in a positive direction until the next reset pulse causes the switch to close and discharge C54. R69 is adjusted during alignment for a charging rate which makes the positive peak of the sawtooth ramp equal to the negative peak. Figure 5.06 shows the horizontal reset pulse and horizontal ramp. (Note: The width of the horizontal reset pulse depends upon the type of CRT controller IC used in the Logic Module. In some cases the width is a bit more than three microseconds rather than the 10 microseconds shown here. Note also that the period for the horizontal ramp in a 48-line unit will be near 42 microseconds rather than the approximately 63 microseconds seen here for a 32-line unit.)

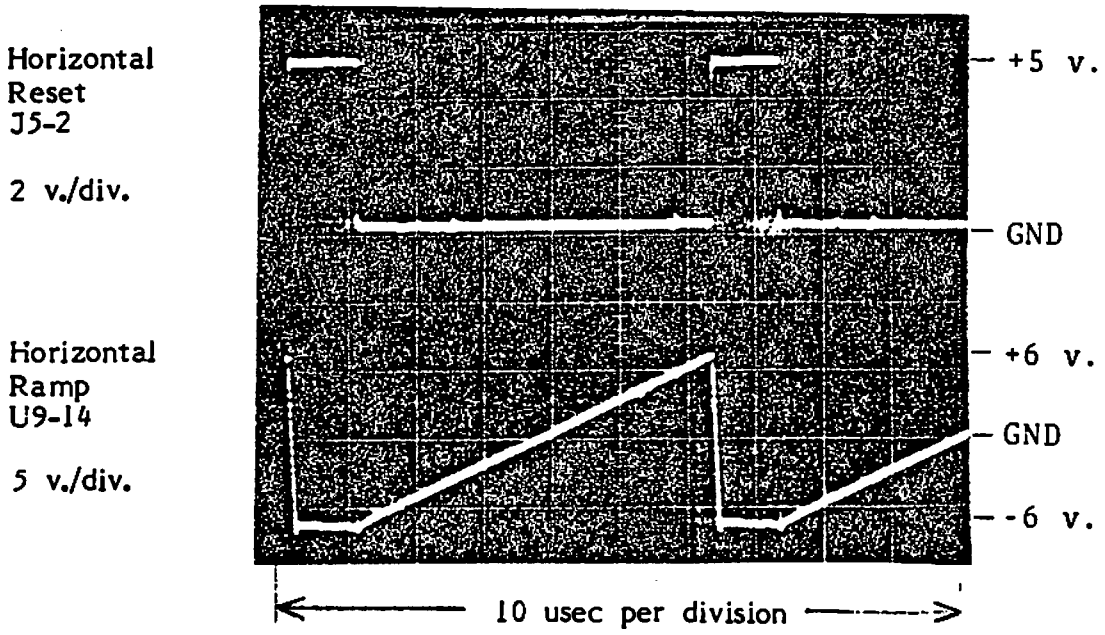


Figure 5.06

The horizontal ramp is connected to both inputs of multiplier chip U16. The output of U16 is the product of the inputs divided by approximately 10 -- in this case, with the horizontal ramp connected to both inputs, the instantaneous ramp voltage squared and divided by 10. Thus the output of U16 is parabolic. If the input ramp is symmetrical -- negative peak and positive peak equal -- the two tips of the parabola will be equal in height. R69 is adjusted during alignment to achieve this result.

The level of this parabola with respect to ground can be adjusted by R80. During alignment R80 is adjusted to set the center point (bottom) of the parabola at ground level. Figure 5.07 shows the horizontal parabola.

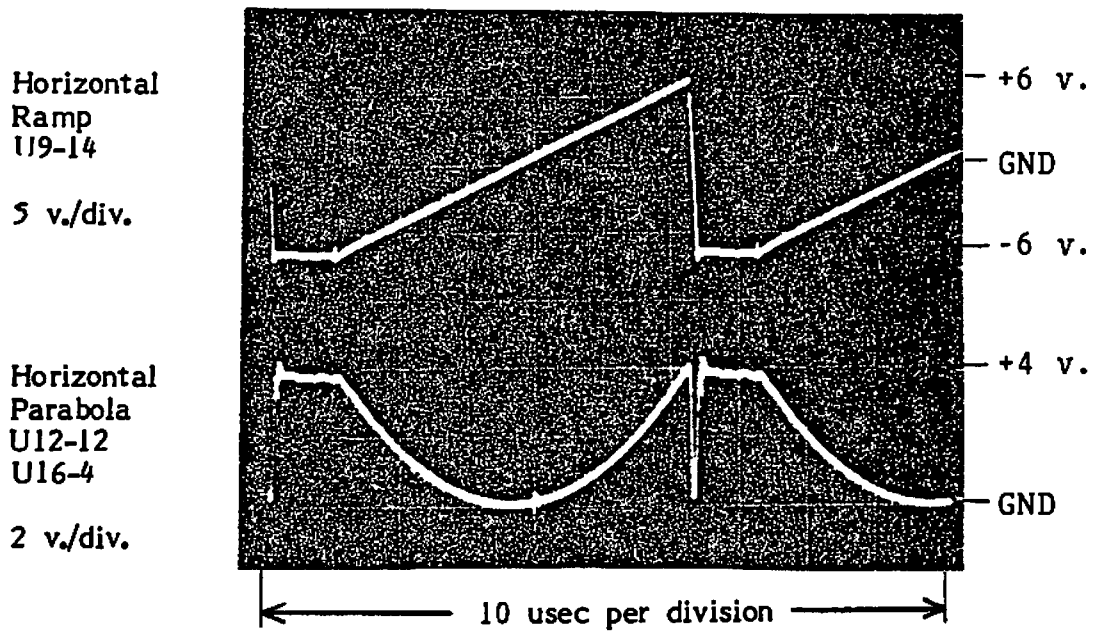


Figure 5.07

This parabola is connected to two inputs of switching chip U12, pins 11 and 12. This "double-pole" section of U12 is controlled by the output of a section of U9. That U9 section, connected as a comparator, compares the horizontal ramp (input at pin 10) to ground. During the negative first half of the ramp the output at U9 pin 8 is negative. The "contact" between U12 terminals 12 and 13 is closed to pass the first half of the horizontal parabola to output connector J12 pin 8. When the ramp crosses ground level to the positive voltage area, the voltage at U9 pin 8 switches quickly to positive. This causes U12 contacts 12-13 to open and and the circuit between pins 11 and 10 to close. The right half of the horizontal parabola is passed to J12 pin 1.

Figure 5.08 shows the comparator output used for switching U12. Figure 5.09 shows the outputs of U12, the leading half of the parabola at terminal 13 and the trailing half at terminal 10.

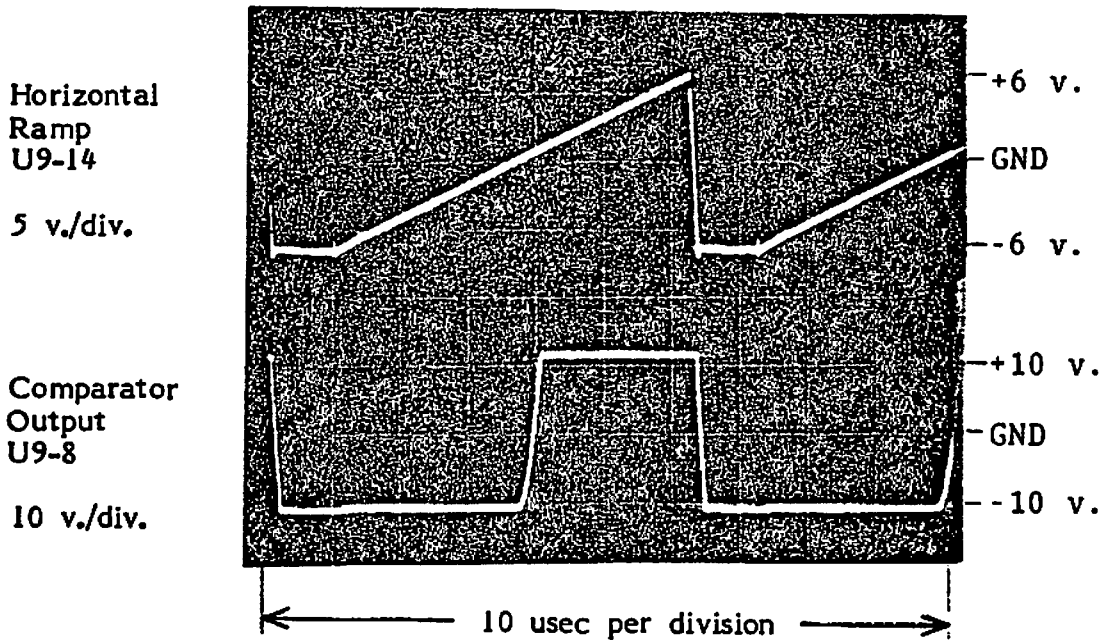


Figure 5.08

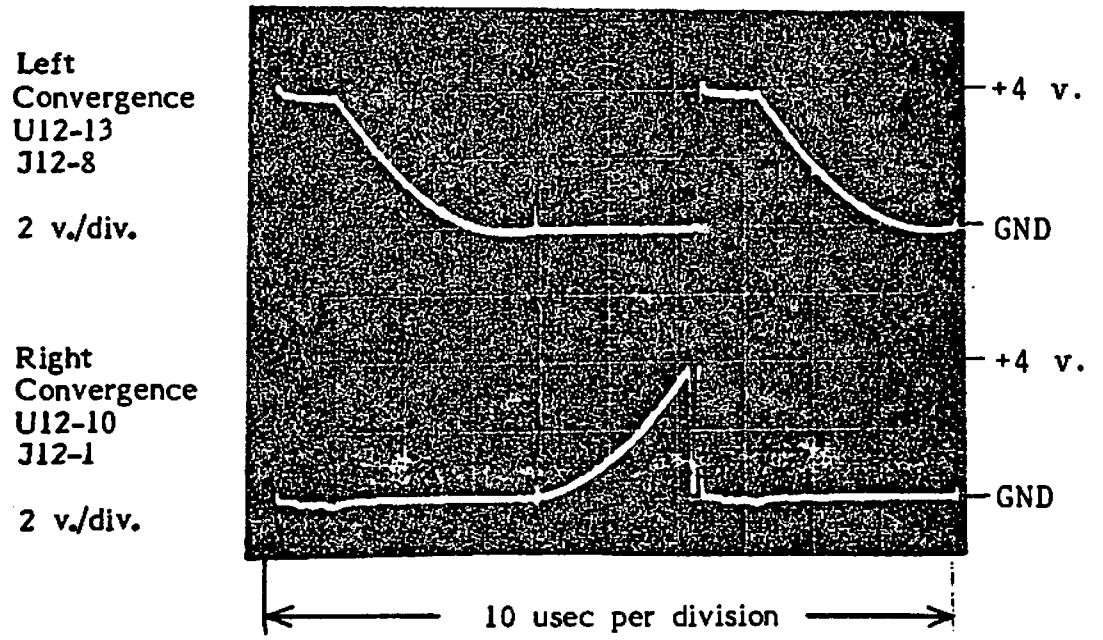


Figure 5.09

The circuit for generation of the vertical ramp and the top and bottom convergence waveforms is similar to that just described for the horizontal waveforms. The principal difference is the size of the ramp capacitor C56. Due to the longer time involved for the vertical ramp, C56 has several times the capacity of C54. The potentiometer for adjusting ramp symmetry, R76, also is larger. The vertical reset pulse from the Digital Module, through R77, causes the circuit between U10 pins 4 and 2 to close and discharge C56. The voltage at U9 pin 1 goes to approximately -6 volts. At the end of the reset pulse the voltage at U9 pin 1 begins its linear increase in a positive direction to reach +6 volts as the next reset pulse occurs. R76 is adjusted to make the positive and negative peaks of the sawtooth ramp equal. Figure 5.10 shows the vertical reset pulse and vertical ramp.

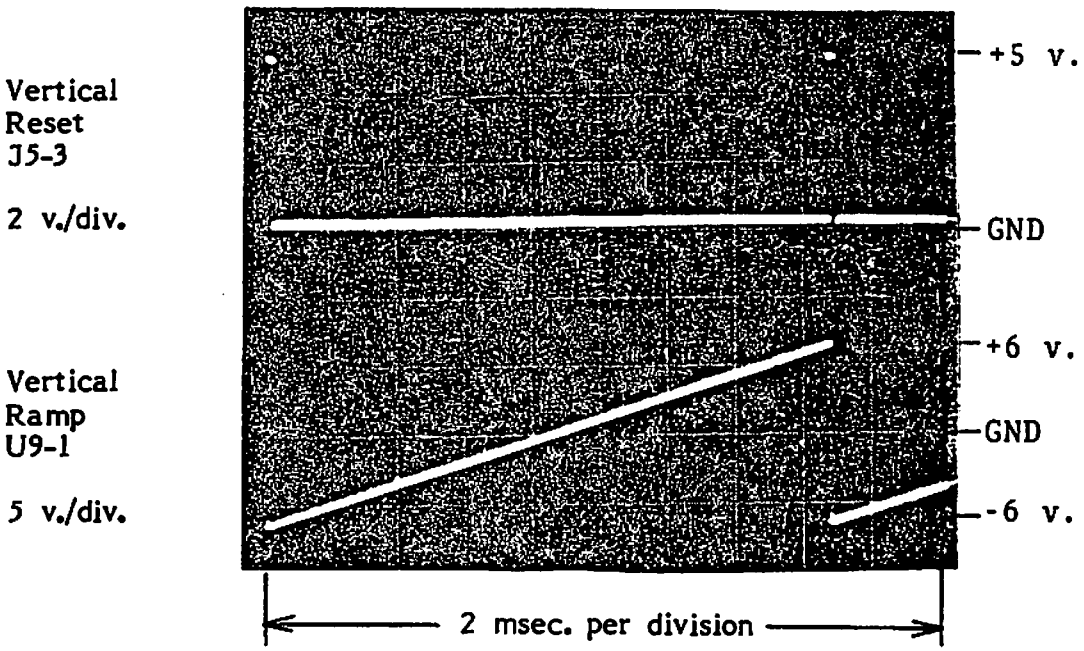


Figure 5.10

This ramp is applied to both inputs of multiplier U11 to produce the vertical parabola at the output of U11. R81 is adjusted to set the DC level of the parabola bottom at ground level. See Figure 5.11.

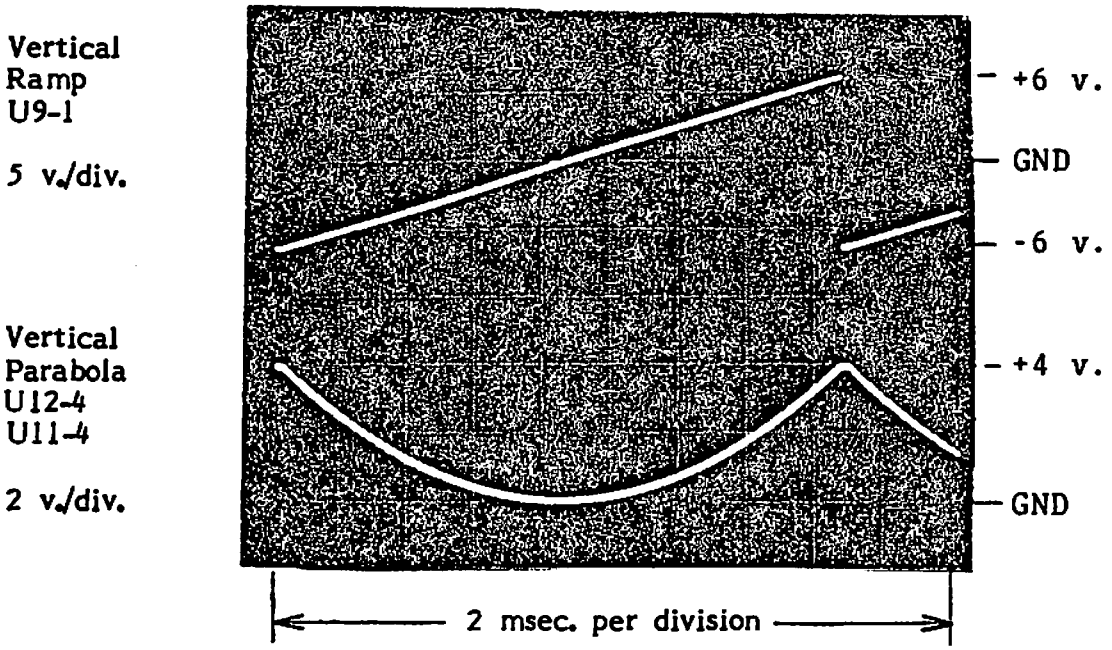


Figure 5.11

The parabola is connected to U12 terminals 3 and 4. The vertical ramp also is applied to a comparator section in U9 to produce a square wave for control of this other switch section in U12. The switching action causes U12 to pass the leading half of the vertical parabola to J12 pin 4 and the trailing half to J12 pin 5, as shown in Figure 5.12.

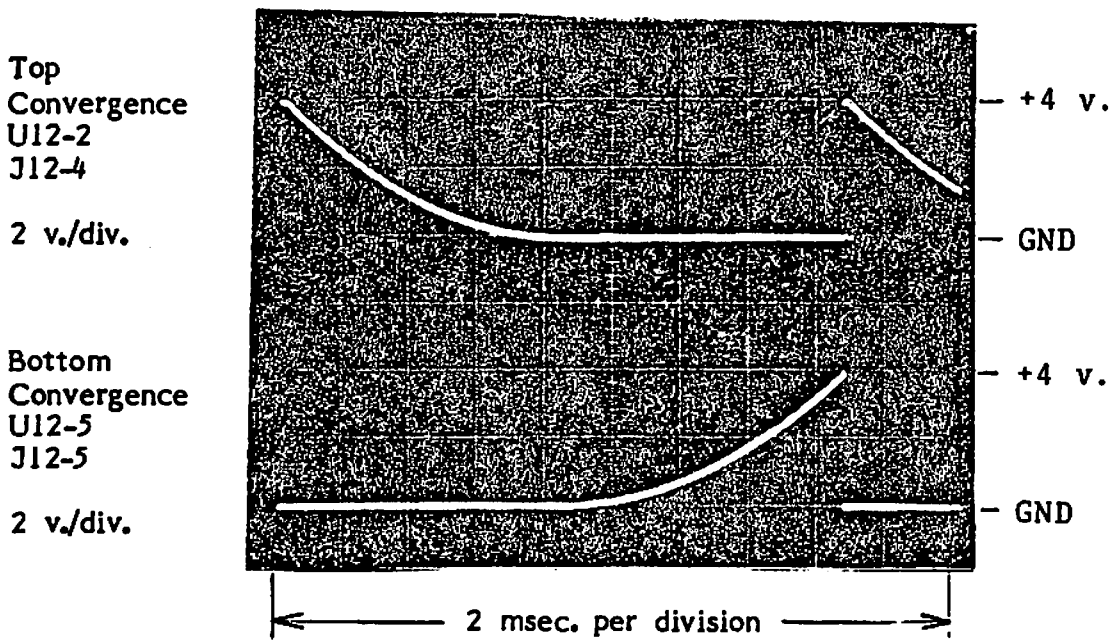


Figure 5.12

For convergence control in the four corners of the screen a pincushion waveform is generated. The horizontal parabola from U16 pins 3 and 4 is connected to one input of multiplier U14. The vertical ramp from U9 pin 1 is connected to the other input of U14. The result is a waveform which, for the period of the vertical ramp, begins with a horizontal parabola inverted and with an amplitude of 3 to 4 volts negative. A series of inverted horizontal parabolas follows, with the amplitudes gradually decreasing to zero. Then follows a series of horizontal parabolas, not inverted, whose amplitudes gradually increase to approximately +3 to +4 volts. See Figure 5.13.

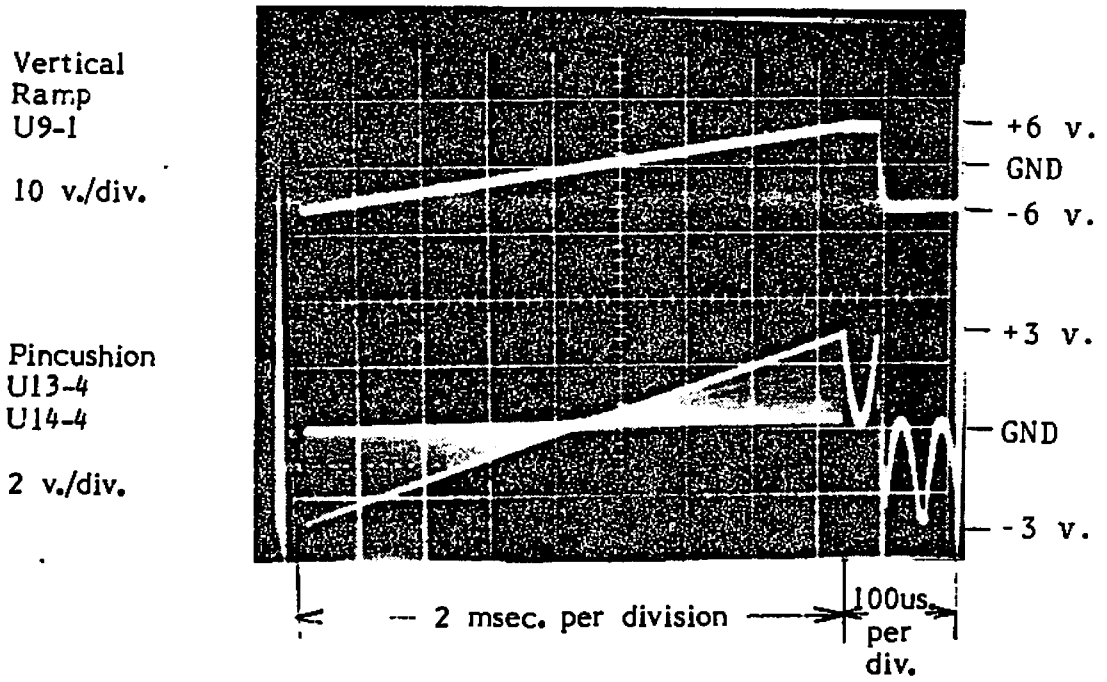


Figure 5.13

This pincushion waveform is connected to terminals 11 and 4 of switch U13. The switching of this section of U13 is controlled by the square wave from U9 pin 7 -- one cycle for each vertical ramp. The leading half of the pincushion waveform is passed to terminal 13 of U13 , the trailing half to terminal 2.

These waveforms are switched further by two sections of U15, under control of the square wave from U9 pin 8 -- at the horizontal frequency. During the first half of each horizontal ramp the first half of the pincushion waveform is passed to J12 pin 6.

Figure 5.14 shows the top left corner convergence waveform. Note in the expanded portion of the pattern that the waveform sweeps up and to the right.

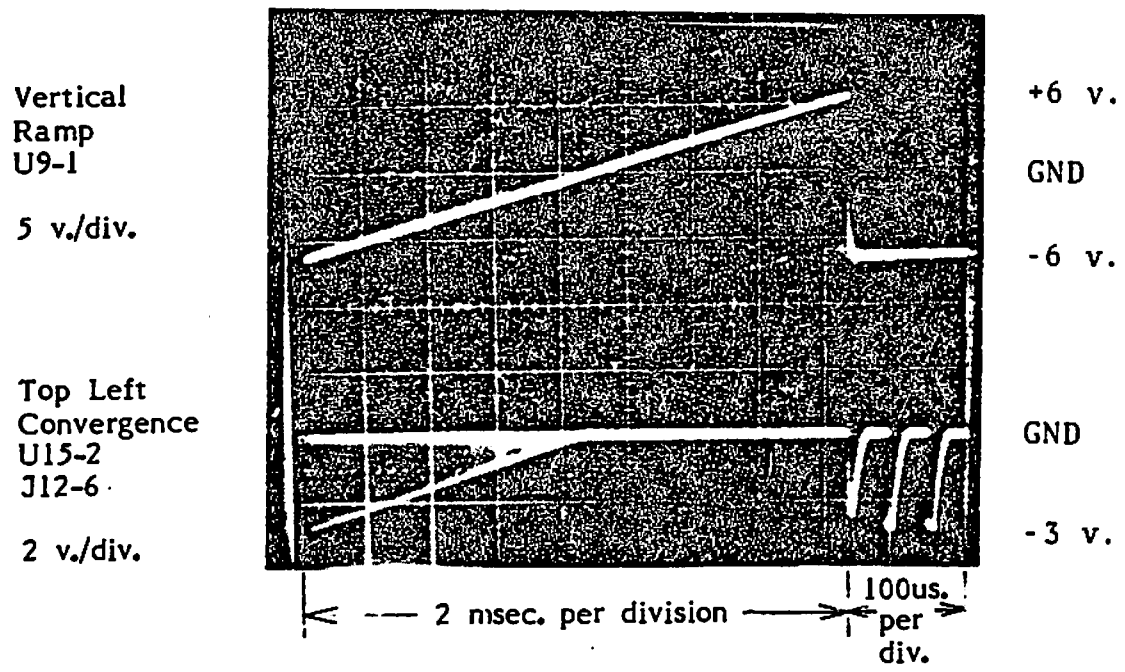


Figure 5.14

During the trailing half of each horizontal ramp this first half of the pincushion waveform is passed to J12 pin 2. See Figure 5.15 for the top right corner convergence waveform, where the expanded portion of the pattern shows the waveform sweeping right and down.

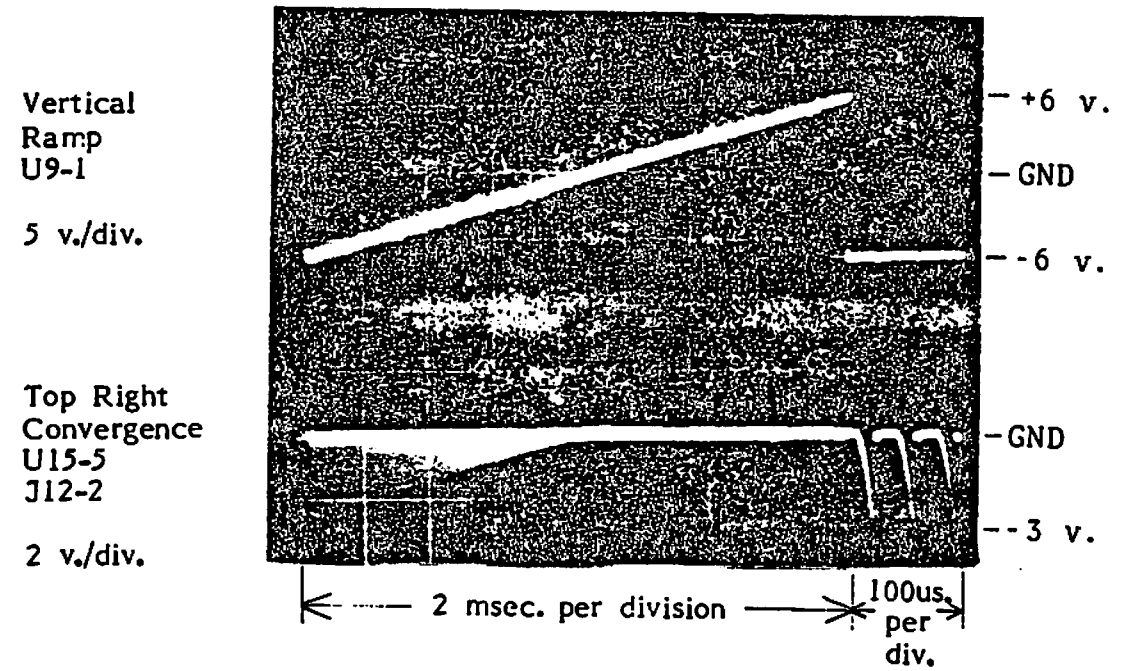


Figure 5.15

In a similar way the other section of U15 passes the second half of the pincushion waveform to J12 pin 7 during the first half of each horizontal ramp and to J12 pin 3 during the trailing half of each horizontal ramp. See Figure 5.16 for the bottom left corner convergence waveform; in the expanded portion of the pattern, the waveform sweeps down and right.

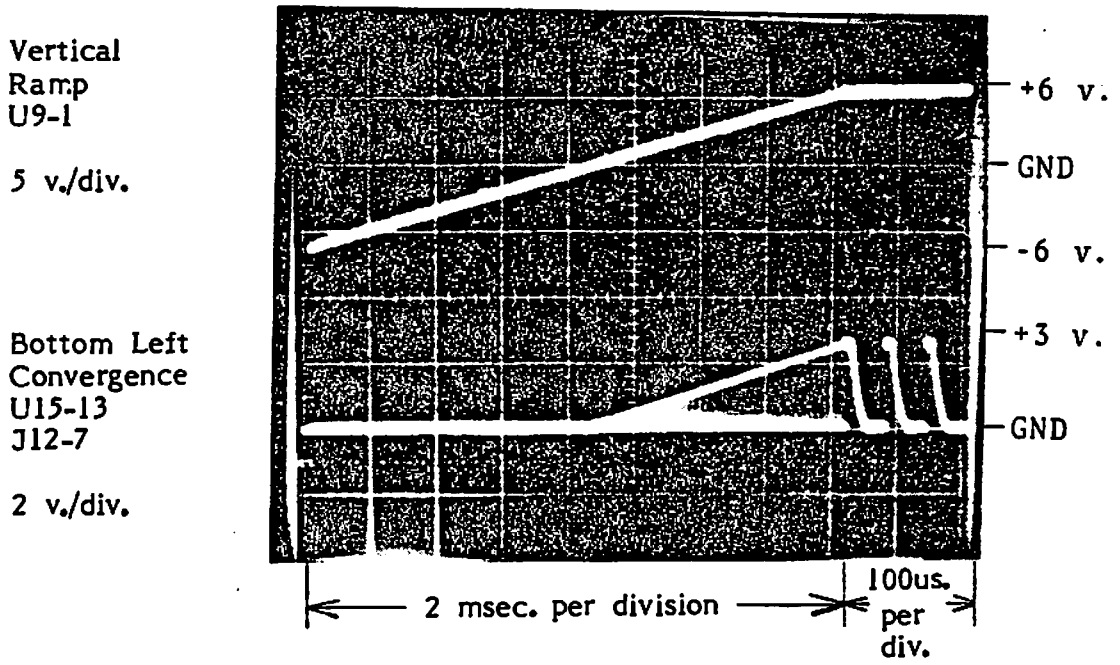


Figure 5.16

In Figure 5.17 the bottom right corner convergence waveform is seen to sweep right and up in the expanded portion of the pattern.

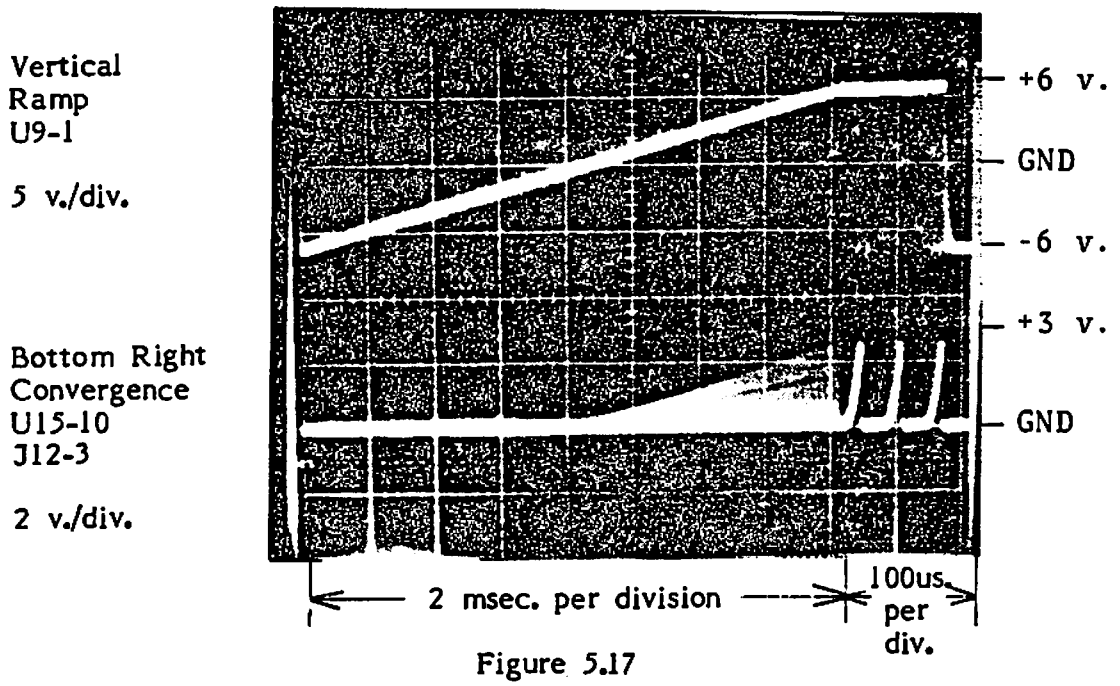


Figure 5.17

The symmetry of the pincushion waveform is adjustable by use of three potentiometers associated with U14. Offset from ground is controlled by R83. Baseline slant is controlled by R82 and vertical symmetry by R84. These are adjusted during alignment to reduce offset and baseline slant to zero and to make the left and right tips of the pincushion waveform equal in amplitude (though opposite is direction), as shown by the sketches in Section IV.

Convergence Amplifiers

The eight convergence waveforms at J12 pins 1 through 8 are connected to the Convergence Module via a flexible cable. The Convergence Module returns three composite waveforms for Red, Blue and Green to J12 pins 9, 15 and 14 respectively. Each of these is amplified by an IC driver SE540. (These driver chips are shown on the right side of the schematic, U17, U19 and U8.) Power voltages for each of these chips are +24 and -24. The SE540 loads are the convergence coils in the CRT yoke. Ground returns are through 10-ohm resistors R99, R94 and R89. There is a path for negative feedback from each terminal of the convergence coils.

Vertical Deflection

The vertical sweep amplifier (see schematic, just left of bottom center) has the vertical ramp A from U9 pin 1 as a principal input. A portion of the ramp voltage is taken from VERTICAL HEIGHT potentiometer R53 and passed through U3 to the inverting input of SE540 driver U2. Use of U3 and a high resistance potentiometer enable the use of a small coupling capacitor for the ramp while maintaining good linearity. U3 pin 6 is connected to U3 pin 2 to give unity voltage gain through U3.

The vertical ramp is inverted by U2. Outputs from terminals 7 and 9, of similar phase, are applied to emitter follower transistors Q13 and Q14 respectively. The terminal 8 output to potentiometer R63 is used to adjust Q13 and Q14 for class AB operation. The combined outputs of Q13 and Q14 control the current through the vertical deflection coil in the CRT yoke. Ground return is through resistor R66. There is a feedback path to the U2 input from each end of the deflection coil.

The sawtooth ramp signal alone would cause vertical deflection at the left and right edges of the screen to be greater than that at the center. The CRT beam travels farther to reach the edges as the sweep is left or right of center horizontally; a constant angle of deflection would result in greater deflection vertically at the screen. See Figure 5.18. Therefore the vertical sweep waveform is modified by the pincushion waveform from U14 pins 3 and 4. This signal B, level adjusted by R54 and applied to the non-inverting input of U2, serves to reduce the vertical sweep signal as the horizontal sweep has the CRT beams either side of center horizontally. VERTICAL PINCUSHION potentiometer R54 is adjusted during alignment to maintain vertical deflection constant during each horizontal scan and give the raster straight edges at the top and bottom.

VERTICAL POSITION potentiometer R57 adjusts the bias of U2 to center the CRT display vertically.

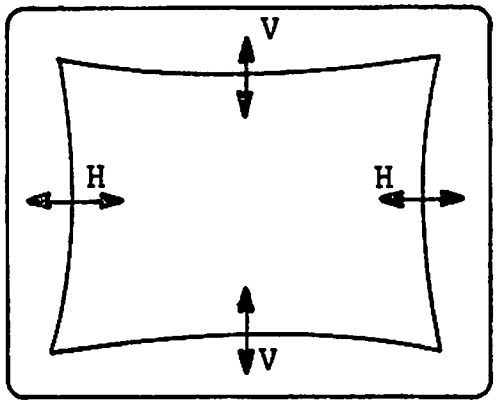


Figure 5.18

Figure 5.19 shows a typical voltage waveform of the vertical sweep amplifier output at J8 pin 2. The effect of pincushion is quite noticeable. The lower waveform in Figure 5.19 shows the average current waveform as seen at J8 pin 1.

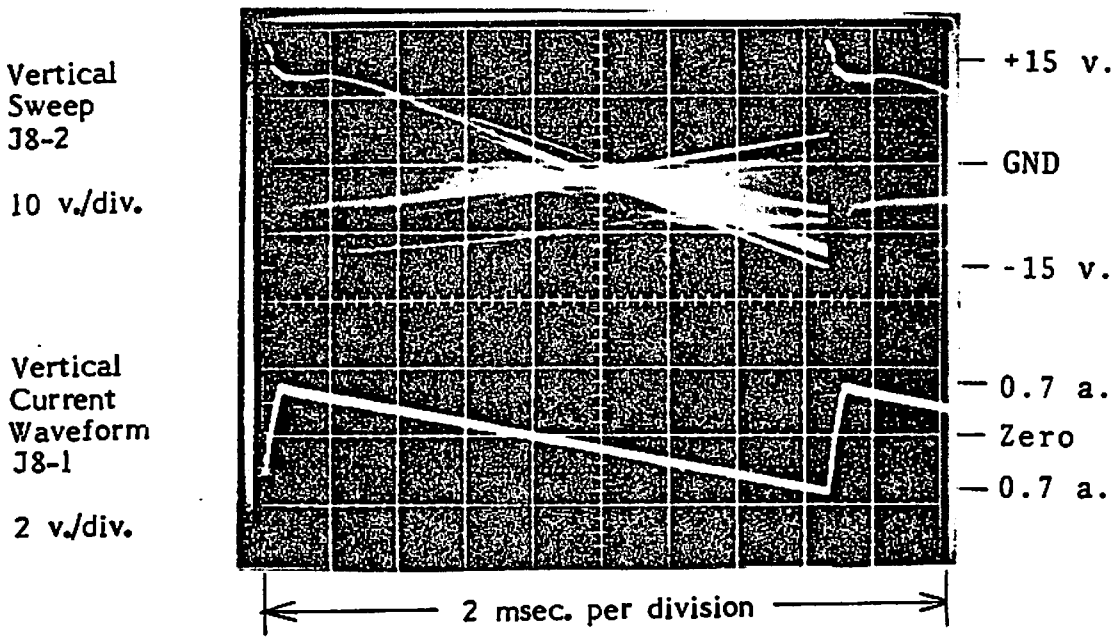


Figure 5.19

Figure 5.20 shows the waveform used to monitor the adjustment of R63. It is taken with the ungrounded oscilloscope's common lead connected to the emitter of Q14 and its probe at the emitter of Q13. R63 is adjusted to put the upper point of the triangular waveform 25 millivolts from "ground", causing Q13-Q14 to be operating just in the Class AB area, very nearly Class B.

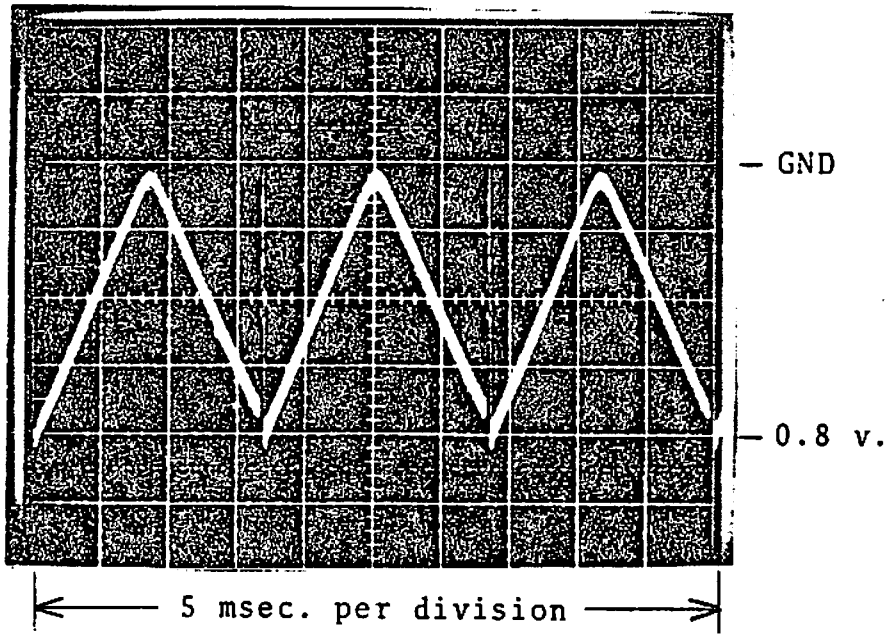


Figure 5.20

This completes the description of the vertical sweep amplifier.

Horizontal Deflection

The horizontal delfection circuit is shown on the left side of the schematic drawing. Horizontal deflection is timed by the horizontal drive pulse from the Digital Module. (The horizontal ramp generated in the convergence waveform circuitry is not used for horizontal deflection.) This drive pulse is a rectangular waveform with a duty cycle near 50%. Its positive rise occurs several characters into the visible portion of the horizontal scan. The trailing edge of the pulse is adjustable (in the Digital Module) for positioning the sweep horizontally. The time relation of Horizontal drive to horizontal reset is shown in Figure 5.21. The end of the visible sweep is near the trailing edge of the positive horizontal drive pulse.

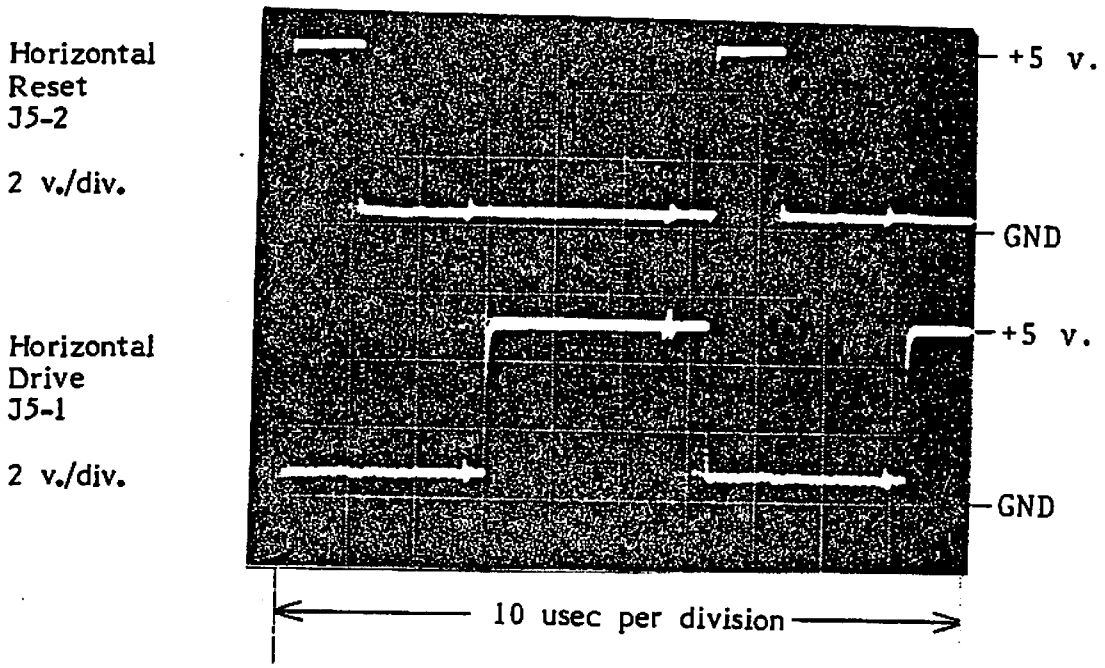


Figure 5.21

The horizontal drive pulse is inverted in a gate in U1 and amplified by transistor Q4. Figure 5.22 shows the output of transistor Q4.

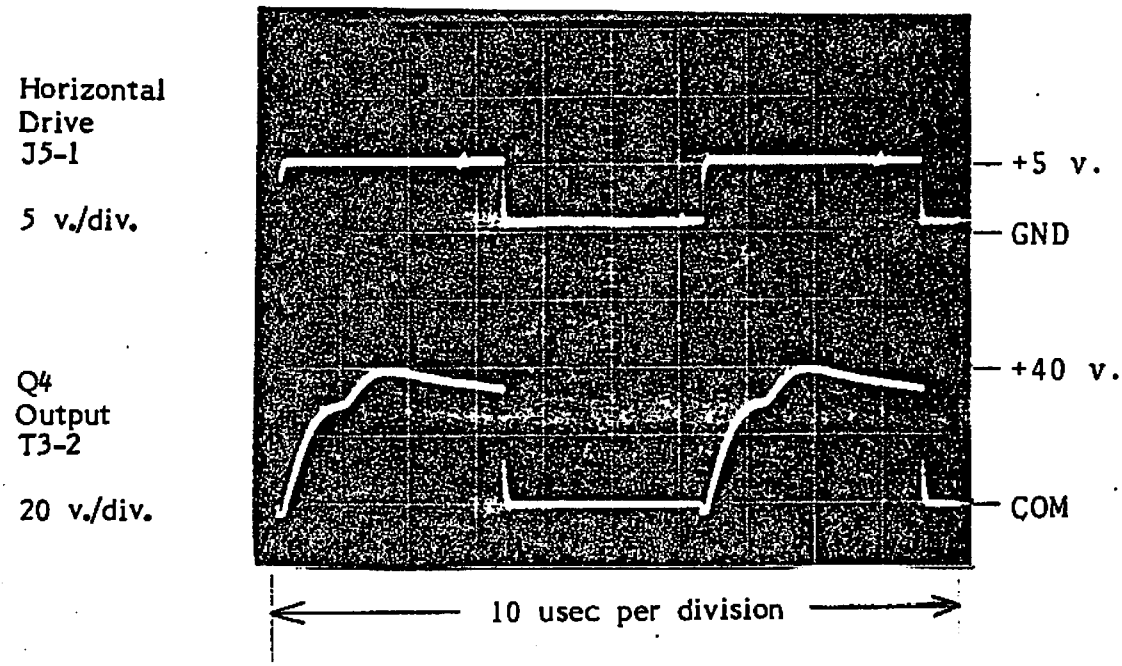


Figure 5.22

The amplified pulse is coupled through transformer T3 to turn on transistor Q9.

NOTE THAT AT THIS POINT THE CIRCUIT IS NO LONGER REFERENCED TO CHASSIS GROUND. UNGROUNDED INSTRUMENTATION MUST BE USED FOR MEASUREMENTS.

Q9 turn-on starts current flow through the flyback transformer T3 primary (terminals 7 and 6) and through the horizontal deflection coil in the CRT yoke. Soon after the end of the drive pulse Q9 turns off and transformer flyback action reverses the current direction for beam retrace. Then, as the beam moves back toward center, the next drive pulse arrives and causes the action to repeat. (The horizontal frequency is approximately 15.6 KHz. for the 64 character/32 line format; for the 80 character/48 line format it is near 23.8 KHz.) Figure 5.23 shows the flyback pulse at the collector of transistor Q9.

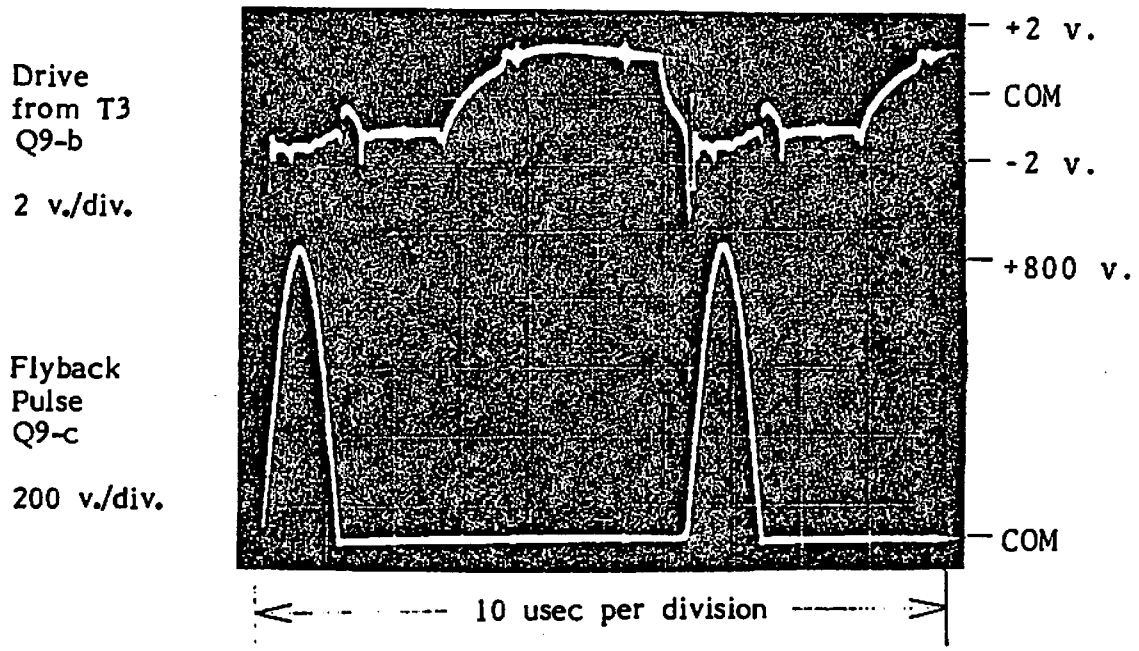


Figure 5.23

The amplitude of the sweep is determined by the voltage available at transformer T3 terminal 7. This is set by the regulatory circuit associated with U5 and Q8. This circuit regulates the voltage across filter capacitor C34 in somewhat the same way that U7 and Q7 regulate the voltage to Q6-c in the low voltage power supply circuit. In this case the SG3524 oscillator frequency is synchronized to the horizontal drive frequency. The horizontal drive pulse is applied through transistor Q2 to U5 pin 3. This shortens the period of the chip's oscillator and increases its frequency to that of the horizontal sweep -- a frequency higher than the free-running frequency set by R31 and C28. Both switched outputs of U5 (pins 12 and 13) are used, so the switching frequency of Q8 is at the horizontal drive frequency.

The sync for U5, developed from the horizontal drive pulse, is shown in Figure 5.24. The U5 output at pin 13 is shown in Figure 5.25. The switched output of transistor Q8 is shown in Figure 5.26.

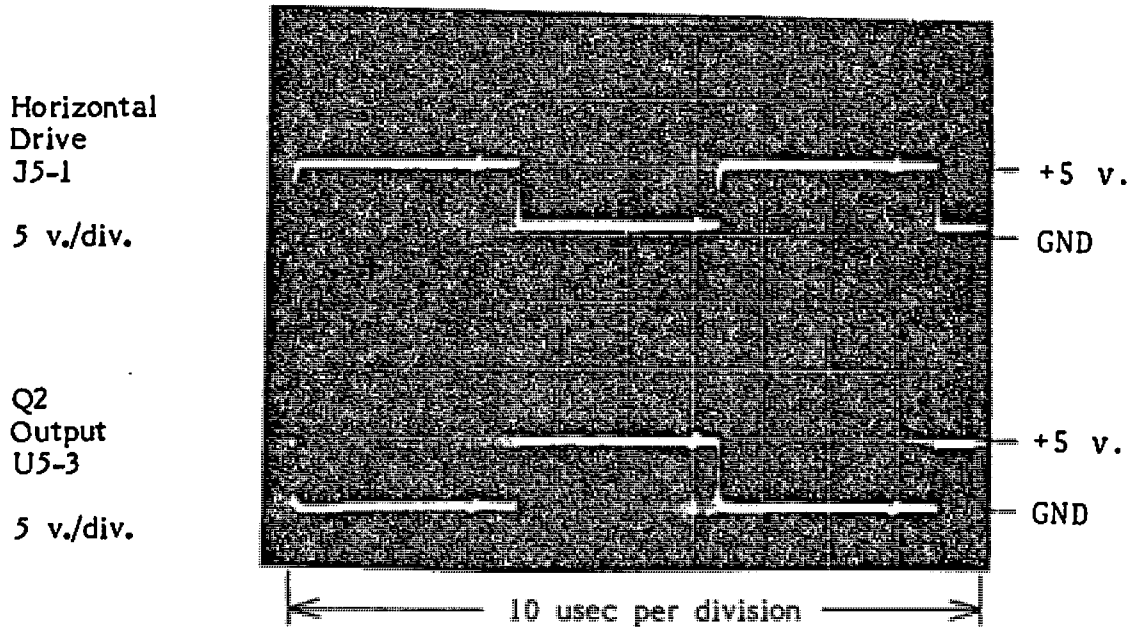


Figure 5.24

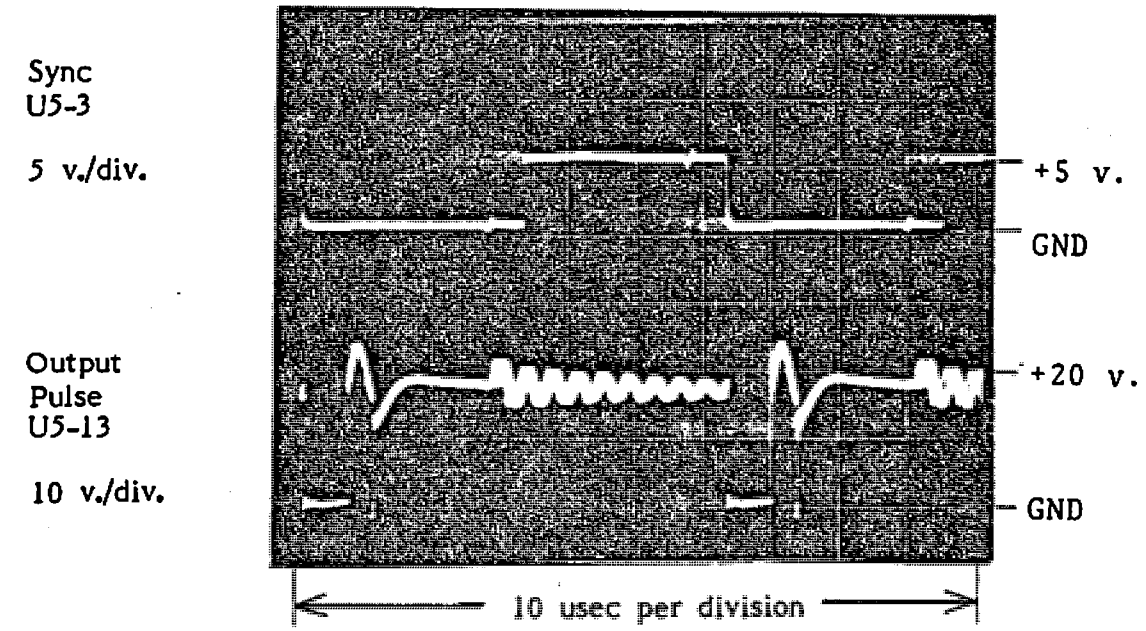


Figure 5.25

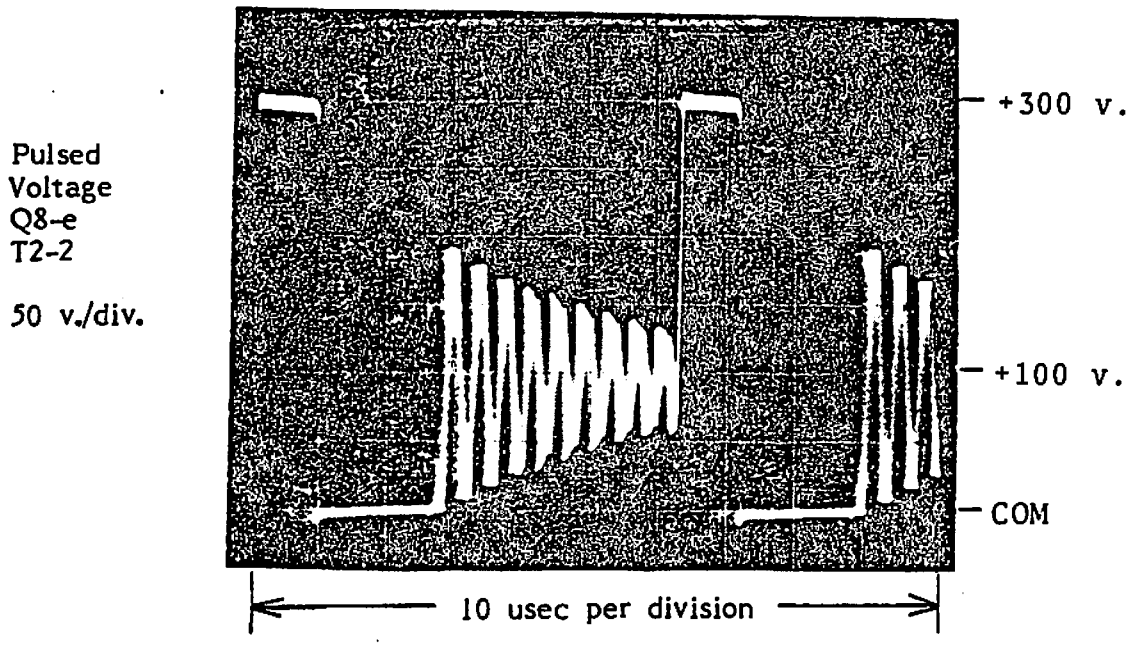


Figure 5.26

A feedback voltage is developed by a full-wave rectifier (CR12 and CR13) connected to a secondary winding of T3. The amount of this feedback is adjustable by potentiometer R35. This HORIZONTAL WIDTH control is adjusted during alignment to obtain the desired display width of 9.5 inches.

As with vertical deflection, the horizontal deflection must be modified to maintain constant deflection at the screen as the CRT beams depart from the screen center (in this case, vertically). To accomplish this the vertical parabola from U11 terminals 3 and 4 is connected as signal D to VERTICAL PINCUSHION potentiometer R39. It is used, through R38, in the feedback to U5 to vary the voltage at FBT1. It also is used through R48 and U4 to modify the horizontal drive pulse. R39 is adjusted to obtain straight vertical sides for the raster.

U4 and Q3 affect the voltage available to the collector circuit of horizontal drive amplifier Q4. U4 sets the bias on Q3; Q3 shares part of the Q4 collector circuit, R50, and thus affects the value of the voltage available to Q4. Potentiometer R46 in the bias circuit of U4 can be used as a sort of vernier control for horizontal positioning. The principal horizontal positioning adjustment in the Digital Module moves the display in discrete character-multiple jumps; R46 provides further control of an analog nature.

The HORIZONTAL WIDTH control R35, in addition to determining the display width, affects the CRT anode voltage. This action is described in the paragraphs following.

Regulated High Voltage DC

Associated with the horizontal deflection circuitry are two additional circuits for generation of the CRT anode voltage, focus voltage and brightness control. One secondary winding of flyback transformer T3 generates a high-voltage flyback pulse which is rectified by a diode to yield the CRT anode voltage. This voltage is set to approximately 25 KV (with reference to chassis ground) when R35 is adjusted for a display width of 9.5 inches. It is maintained at this value by the regulatory action of U5 and Q8.

A voltage divider is connected in series between the CRT anode cap and the FOCUS potentiometer located on the rear panel of the Analog Module. A lead from the voltage divider connects the focus voltage to the CRT socket on the Video Module. As part of the divider circuit, the FOCUS control adjusts the level of this focus voltage.

Another secondary winding (terminals 1 and 6) in the flyback transformer supplies the CRT filament or heater voltage, which is connected through the CRT socket on the Video Module.

For control of brightness and color mix, the flyback pulse at Q9-collector is coupled through C37 to rectifier diodes CR10 amd CR11. The resulting DC is filtered by C38-R40-C39. This voltage is used in the Video Module for individual control of the brightness of the three primary colors. For overall brightness control the voltage is used by the Q12 circuit to set the bias on the CRT grids. BRIGHTNESS control R113 is used to adjust the bias of Q12 and thus set the bias on the CRT grids.

Video Gates

The three video signals, Red, Green and Blue, from the Digital Module's display generator section are brought to the inputs of NAND buffers in U1 (lower left corner of schematic). The inverted video pulses at the gate outputs, with amplitudes of 4 or 5 volts p-p, are connected to amplifiers in the Video Module.

Interconnections

Leads and cables between the Analog Module and other modules are connectorized at one or both ends for easy disassembly. Deflection and convergence leads from the CRT yoke plug into jacks on the upper side of the Analog board. Cables for power and video from the Analog board to the Video Module have sockets which mate with plugs on the Video board. Cables between Analog and Digital Modules in the 32-line unit have sockets to mate with jacks on the Digital board. (An opening in the Analog board provides access to the plugs. Whenever corrective maintenance work involving the power supplies has been performed, socket J6 should be disconnected from the Digital Module to remove power until the low voltage supplies have been adjusted.)

This completes the description of the Analog Module. For adjustment procedures, see Section IV Alignment.

CONVERGENCE MODULE

The Convergence Module consists of nine sets of three potentiometers for nine-sector convergence adjustment and three summing amplifiers (one for each color). The components are mounted on a PCB 2 5/8" x 4 1/8" which is located in a front panel recess behind a snap-off cover -- just above the right side of the keyboard. A flat flexible cable with plugs connects the module to the Analog Module.

One of the eight different convergence waveforms developed in the Analog Module is applied to each of eight of the sets of controls. The centrally located set of controls for center screen convergence has -12 VDC as input. The output of one potentiometer in each of the nine sets is applied to one of the summing amplifiers in UA1. One section of UA1 sums the inputs for Green convergence, another section sums those for Blue convergence, and a third those for Red. The outputs of these three amplifiers are returned to the Analog Module as inputs to the three convergence coil drivers.

The physical locations of the nine sets of controls follow the same pattern as that of the screen areas controlled -- see diagrams in Alignment Section IV.

VIDEO DRIVER MODULE

The Video Driver Module contains three video amplifiers, three brightness controls and the socket for the cathode ray tube. The components are mounted on a printed circuit board 6" x 2 3/8". The CRT socket is used to mount the module to the base of the CRT. Component locations are shown on Assembly Drawing 101170 and the circuit is shown on Schematic Drawing 101174.

The module has two jacks for connections to the Analog and Digital Modules. Power voltages from the Analog Module via a cable that mates with J1 on the Video PCB include +5V, -12v, +48V and +200V DC and 6.3 VAC. The cathode return for all three CRT cathodes is through 10K resistor R4 to J1 pin 2. (A circuit in the Analog Module establishes the bias on this cathode return lead.)

The +200V is connected to the three brightness controls R19, R17 and R18 for Blue, Green and Red respectively. The outputs of these three potentiometers are connected through 10K resistors to the CRT screen grids by way of the CRT socket. Each pot output has a by-pass to ground.

Focus voltage is connected through a separate lead from the CRT socket. A connector on this lead mates with a connector on the lead from the focus circuit voltage divider in the Analog Module.

A ground strap mates with a grounding tab on the Video PCB, connecting CRT socket pin 10 to the CRT grounding springs and the Analog frame.

Video signals for Red, Blue and Green are generated in the Digital Module, brought through gates in the Analog Module and brought into the Video Module at J2 on the Video PCB. Each of the three video amplifiers has one field effect transistor. In the GREEN amplifier (toward the bottom of the schematic) the input video is applied to the gate of FET Q3. The load of Q3 has frequency compensation (L1) to provide a bandwidth of some 50 MHz. The amplified video, with an amplitude of 40 volts p-p, is connected through 470-ohm resistor R12 to the CRT socket pin for the Green cathode. The supply for Q3 is +48V. The RED and BLUE amplifiers are similar to the GREEN. Figure 5.27 shows video signals input from the Logic Module through the Analog Module and the output from the Video Module to the CRT.

During alignment the individual BRIGHTNESS controls R17, R18 and R19 are adjusted in conjunction with overall BRIGHTNESS control R75 (mounted on the Analog rear panel) to give the desired color mix at a comfortable viewing level.

NOTE: In some units there is an IC on the Video Module for the video input gates. In these cases the video from the Logic Module is brought directly to the Video Module instead of being passed through the gates in U1 on the Analog Module.

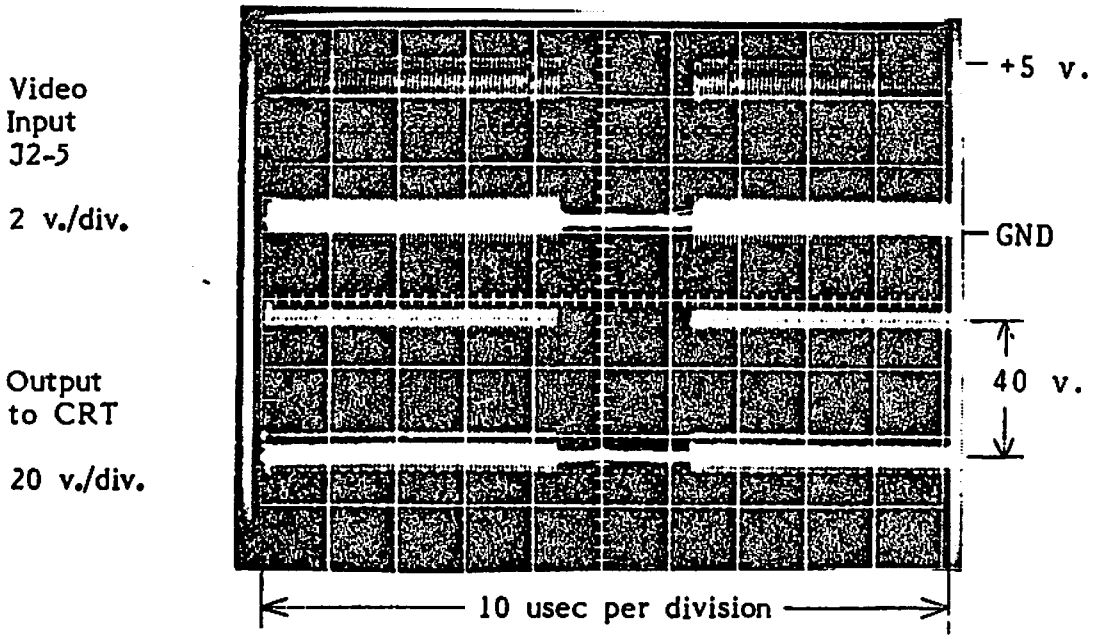

Video
Input
J2-5
2 v./div.
Output
to CRT
20 v./div.
+5 v.
GND
40 v.
10 usec per division

Figure 5.27

DIGITAL MODULE - 3621

The Digital Module (Logic Board) is mounted in the lower part of the cabinet underneath the Analog Module. It receives input data and, together with the software, processes it for CRT display or for serial transmission to the Disk Controller or to the outside world. Schematic Drawing 100961 shows the circuit which, for discussion purposes, may be treated as a microcomputer and a display generator.

The microcomputer, occupying the left two-thirds of the drawing, includes the 8080 Central Processing Unit (UA2), a Clock Generator (UB1), a Multifunction Input/Output Unit (UD2), Read-Only Memory (UA4-UA7), CRT Refresh Random Access Memory (UD4-UD11), user Random Access Memory (UB4-UB11) when included in the configuration, and several other devices for selection and control of data processing functions. (Terminals without user RAM have a small amount of static RAM on a plug-in board.) A Data Bus and an Address Bus provide much of the interconnection.

The display generator, shown on the right one-third of the schematic drawing, includes the 5027 CRT Controller (UF9), Character Generator (UF6-UF7). Character, Status and Color Latches (UE6, UE5, UE4), Shift Register (UF5), Color PROM (UG5), and several additional devices involved in the selection and timing of signals for the CRT display. The CRT Refresh RAM (UD4-UD11) also is part of the display generator.

Data is received through either the Serial I/O Ports or the Keyboard. It is processed by the microprocessor and software and routed via the control and data buses to the appropriate circuit. If it is data to be presented on the screen, it is placed in the CRT Refresh RAM along with an appropriate control word to identify the color, blink and graphics status.

Once in Refresh RAM, the data is presented to the display generator circuitry. Here the first of two memory words is processed into an ASCII character or graphics dot pattern; the second word is processed simultaneously into color, blink and graphics identifier information. The resulting serial output of color video information -- red, green, blue -- is coordinated with horizontal and vertical synchronizing signals to synchronize the serial output information with the CRT horizontal and vertical sweep signals generated in the Analog Module.

Microprocessor

The 8080 CPU and its associated 8224 Clock Generator, 74S438 Bus Driver and Controller and the 5501 I/O Controller make up the heart of the Digital Module computer functions.

The 8080 CPU is a general purpose microprocessor that can handle 8-bit words, has a repertoire of 78 instructions and can address up to 64K of memory through the address bus. Appendix A at the back of this manual details the features of this integrated circuit chip.

The 8224 Clock Generator includes a 17.9712 MHz. oscillator, controlled by crystal Y1, and generates timing pulses O1 and O2 at one-ninth the crystal frequency. (The 17.9712 MHz. output from terminal 12 is routed to a number of other units for timing purposes. These will be mentioned as the other units are discussed.)

The 8-line data I/O port of the 8080 CPU connects in parallel to the 74S438 Bus Driver/Controller and the 5501 I/O Controller. All data to or from the 8080 CPU passes through one of these two units.

The 5501 I/O Controller passes data to and from the Keyboard and the Disk Controller (and the Data Modem, if used). It handles both serial and parallel data. Data to be sent to the Disk Controller or the Data Modem are converted to serial form and transmitted through the 1488 Line Driver (UG1). Data bits 05 and 05 from the 5501, applied to a NAND gate in UF2 (74LS00), enable transmission to the designated unit. Serial data from the Disk or Modem come through the 1489 Line Receiver (UD1), also controlled by data bits 04 and 05 from the 5501. See table below.

UF2				UD1		Built-in	Add-on	Modem
12	13	11	Q2	8	Q1	Disk	Disk	
L	L	H	ON	L	OFF	ON	ON	OFF
L	H	H	ON	L	OFF	ON	OFF	OFF
H	L	H	ON	L	OFF	OFF	ON	OFF
H	H	L	OFF	H	ON	OFF	OFF	ON

Thus when either of bits 04 and 05 is low, the Line Driver and Receiver sections associated withe the Disk Controller are enabled. The outputs of the sections associated with the Modem are held high. When both bits are high, the reverse is true. Bit 04 low causes the resident Disk Drive to run. Bit 05 low causes the add-on Disk Drive (connected to a branch of the keyboard cable) to run.

Parallel outputs O0-O7 from the 5501, passed through the 81LS95 Octal Buffer (UF1) without inversion, serve both as controls for the Disk Controller and as inputs to the Keyboard. The Keyboard returns 12 lines of information to the Logic Board. Eight of these are multiplexed by the 74LS157 Quadruple 2-line-to-1-line Multiplexer (UE1) onto four lines. These, with four of the original 12, make up an 8-line parallel input to the 5501. The Keyboard also has a RESET input to the Logic Board to reset the microprocessor to its initial condition.

The operation of the 5501 I/O Controller is determined by address bits A0-A3 from the 8080 CPU. Appendix B provides considerable detail concerning the TMS 5501 Multifunction Input/Output Device.

The 74S438 Bus Driver/Controller handles all other parallel data transfers between the 8080 CPU and a variety of units, including the user Random Access Memory, Read-Only Memory, add-on RAM and ROM, CRT Controller and CRT Refresh Random Access Memory. The 74S438 reads the status off the 8080 I/O Port data to determine the action to be taken.

As a bus driver, the 74S438 provides isolation between the 8080 Data Bus and the memories. As a controller, it issues the Memory Read/Write and Input/Output Read/Write commands.

The System Driven Data Bus originates at the 74S438 Bus Driver/Controller terminals DB0-DB7. From there (Schematic Drawing 100961, upper left corner) its eight lines, designated D0-D7, connect in parallel to the following units:

Description	Function
1) 50-pin bus J3 for add-on units	I/O Data
2) Connector J8 for 16K user RAM (or scratch pad RAM)	I/O Data
3) 16K user RAM (UB4-UB11) when present	I/O Data
4) 81LS95 Octal Buffer (UE7)	Refresh RAM Output Data
5) 4K Refresh RAM (UD4-UD11)	Input Data to Refresh RAM
6) 82S123 I/O PROM (UA1) when present	CRT Controller Data
7) 16K ROM (UA4-UA7)	ROM Output Data
8) Connector J9 for add-on ROM	Output Data
9) 5027 CRT Controller (UF9)	Input Data for CRT Control (and I/O for Cursor Data)

The CRT Refresh RAM output data, in addition to being connected to the system driven data bus through Octal Buffer UE7, is connected to the 74LS377 Character Latch UE6 and Status Latch UE5.

The Address Bus is the route over which the 8080 CPU addresses the various memories and I/O ports. This 16-bit parallel data bus originates at the A0-A15 terminals of the 8080 CPU (near upper left of Schematic Drawing 100961) and extends in whole or in part to the following:

Description	Bits Used
1) 50-pin Bus J3 for add-on units	A0-A15
2) 3242 Address Multiplexer/Refresh Counter (UA3) for addressing user RAM (or to scratch pad static RAM in some terminals)	A0-A13
3) 82S129 Address Decoder/Timer (UE2)	A13-A15
4) 82S123 I/O PROM (UA1)	A0-A4
5) 82S129 System Decoder (UF3)	A13-A15
6) 5501 I/O Controller (UD2)	A0-A3
7) 82S123 ROM/PROM Decoder (UB3)	A11-A14
8) 16K ROM (UA4-UA7)	A0-A12
9) A NAND gate in 74LS00 (UF2)	A7 only
10) Connector J9 for add-on ROM	A0-A11
11) 74LS153 Multiplexers (UD12, UE9, UE8) for CRT Refresh RAM address	A0-A11
12) 5027 CRT Controller (UF9)	A8-A11
13) 82S131 CPU & Horizontal Decoder (UF8)	A12 only

(Some address inputs to the 82S123, 82S129 and 82S131 PROMs come from other sources.)

The Digital Module uses several types of Programmed Read-Only Memories. Four PROMs are used for control purposes in the microcomputer portion.

The 82S129 System Decoder (UF3) is a 256x4 PROM. The 4-bit word output from its memory enables certain logic functions:

- D0 is the Chip Enable for the 5501 I/O Controller UD2.
- D1 is the DBIN signal to the 74S438 Bus Driver/Controller UB2 to indicate whether the 8080 Data Bus is in an input mode (DBIN high) or an output mode (DBIN low).
- D2 is part of the address to ROM/PROM Decoder UB3, directing use of the Read-Only Memory.
- D3 is the Chip Select signal to the 5027 CRT Controller and part of the address to the CPU & Horizontal Decoder UF8.

The required 8-bit address to the System Decoder comes from several sources:

A0 is the 8080 DBIN signal.
A1 is the I/O R signal from the 74S438 Bus Driver/Controller.
A2 and A3 are the D6 and D4 bits (advance I/O R and I/O W) from the 74S438, passed through inverters in UC1.
A4, A5 and A6 are address bits A13-A15 from the 8080.
A7 is the MR signal from the 74S438.

The 82S129 Address Decoder & Timer (UE2) is a 256x4 tri-state output PROM which provides the decoding and timing functions for the user RAM. Part of its 8-bit address comes from the Address Bus (bits A13-A15). Two bits are the Memory Read and Memory Write commands from the 74S438 Bus Driver/Controller. One bit is the O2 Clock (TTL level). One is the 8080's WR signal. The remaining bit is the Refresh Signal from the second flip-flop in a 74LS74 (UG2, terminals 8-13). The 4-bit words from memory are involved in RAM functions:

D0 is passed through two Schmitt triggers in UD3 to yield the Column Address Strobe to the user RAM on the plug-in board.
D1 supplies the Refresh Enable and Count inputs to Address Multiplexer UA3.
D2 through a Schmitt trigger in UD3 supplies the Row Address Strobe to all of the user RAM. Through another Schmitt trigger it supplies the Row Enable signal to Address Multiplexer UA3.
D3 is passed through two Schmitt triggers to yield the Column Address Strobe to the user RAM on the main board.

Thus when the address issued by the 8080 CPU indicates access to RAM -- for either Read or Write -- the Address Decoder & Timer PROM enables the Address Multiplexer UA3 and initiates the generation of strobes to the selected Random Access Memory.

The 3242 Address Multiplexer/Refresh Counter (UA3) receives 14 address bits from the 8080 CPU. It multiplexes these into seven outputs (O0-O6). These outputs make up the row/column address inputs for the user RAM. (In terminals with no user RAM the 3242 and some associated circuitry are omitted.)

The Zero Detect output (terminal 15) is an input to one of the monostable multivibrators in 74LS123 (UG4), which times the Refresh Signal. When the 64 (or 128) cycles of refresh have been completed, Zero Detect goes low to trigger the one-shot multivibrator. When it times out in a bit under 1 ms., a high is generated at terminal 12. This high is applied to the terminal 12 D input of a flip-flop in UG2 and is passed on to terminal 9 on the next low-high transition of the 8224 Clock Generator 2 (TTL) signal. This causes the Address Decoder & Timer UE2 to initiate another refresh cycle with high at D1 and at D2.

The Count and Refresh Enable inputs for the 3242 come from the 82S129 Address Decoder and Time (UE2), which also provides the Row Enable signal to the 3242. When terminal 3 of the 3242 is made high, the multiplexer outputs are row addresses; when it is low, the outputs are column addresses.

The User Random Access Memory included in the 3621 Intecolor is made up of 16 one-bit-wide Dynamic RAM (UB4-UB11, plus 8 more IC's on the plug-in board). One chip in each of the two sets of eight supplies one bit of the 8-bit word to be written into or read from memory. The memory cells within are arranged in a matrix of rows and columns. The 14 address bits required to identify a particular cell in the array have been multiplexed on 7 address lines and come into the RAM chips as 7 row address bits followed by 7 column address bits. RAS (Row Address Strobe) and CAS (Column Address Strobe) serve to latch the address into the chip. If data on the Data Bus (connected to chip inputs) is to be written into memory, a negative transition on Write (MW) causes this to occur. If MW is maintained high, data is retrieved from memory and put on the Data Bus.

The Dynamic RAM memory cells require refresh within 2 ms. intervals to maintain their data. Refresh occurs during each memory cycle. Refresh also occurs every millisecond or less, as described earlier in the paragraphs relating to the 3242 Address Multiplexer/Refresh Counter. A memory output from UE2 causes a Schmitt trigger in UD3 to generate the RAS required to refresh the RAM cells. (Refresh takes place during any cycle in which RAS occurs; and when RAS is received without CAS, the memory state is not affected.) Refresh requires 32 us. (64 us. for 128 cycles) for completion.

Some configurations in the 3600 Series have no dynamic user RAM and thus do not need the refresh circuitry. Other configurations may have less than the 32K maximum dynamic RAM.

In units such as the 3621 which have more than 16K of user RAM, a plug-in board is mounted in J8. The plug-in PCB has eight one-bit-wide dynamic RAM chips. In the 3621 these are 16Kx1 4116's. Capacitors for power source by-passing are included on the board adjacent to the chips.

The plug-in RAM is addressed through the 3242 Address Multiplexer/Refresh Counter (UA3) in parallel with the RAM on the main board. The output of the RAM Address Decoder (UE2) provides the Row Address Strobe for the plug-in board in parallel with the chips on the main board. A separate output of this decoder provides the Column Address Strobe to the plug-in board when the address indicates its selection. The MW signal from the Bus Driver/Controller (UB2) indicates whether data on the Data Bus is to be written into memory or data in memory is to be read onto the Data Bus.

In terminal configurations having no user RAM, the plug-in RAM board is used for mounting a small amount of static RAM used as scratch-pad for internal operations. In these configurations neither address multiplexing nor refresh is required. The static RAM is addressed directly by the CPU.

Connectors at each end of the plug-in board mate with the two J8 connectors on the Digital Module. The terminal pins are numbered. Note that the end of the plug-in with terminals 1 through 12 mates with the connector nearer the edge of the main board. Power should be OFF when the plug-in is mated with the main board.

The 82S123 I/O PROM (UA1) is a 32x8 PROM whose 8-bit words, when read from memory, are delivered on the Data Bus for 5027 CRT Controller start up. The chip is enabled by a combination of the I/OR signal from the 74S438 Bus Driver/Controller and the A7 bit from the Address Bus. The negative I/OR transition causes an inverter in UC1 to apply a high to one input of a NAND gate in UF2. If the A7 address bit also is high, the gate output goes low to provide the CE for UA1. Address Bus bits A0-A4 cause the appropriate 8-bit word to be read onto the Data Bus.

In some Intecolor units, where the 5027 CRT Controller is masked for a particular type of operation, UA1 is not required.

The 82S123 ROM/PROM Decoder (UB3) is a 32x8 PROM whose 8-bit output from memory provides a Chip Select to one of the ROM chips UA4-UA7 or one of the optional add-on ROM at J9 when ROM is addressed.

One of the five address bits has an option connection to ground or +5V. Normally this input is connected to Address Bus bit A11. The optional connections are provided for possible shift to different software. Three inputs are Address Bus bits A12-A14. The fifth input is from the System Decoder UF3. When ROM is addressed by the 8080 CPU to read data onto the Data Bus, the ROM/PROM Decoder enables the selected ROM chip.

The Read-Only Memory (UA4-UA7) resident in a 3600-Series Intecolor unit varies with the type of configuration. Normally up to 16K 8-bit words find storage space on the main board. However, use of different types of ROM chips may require changes in the option patches associated with the power voltages, address inputs and chip select leads. The following table shows the patches for a number of types of chips.

INPUT →		+12	-5	A12	A10			CS		GND	A11
PATCH NO. →		1	2	3	4	5	6	7	8	9	10
ROM CHIP	2708	X	X					X		X	
	2716	X	X				X		X		
	4732					X		X			X
	9216	X			X			X		X	
	36000			X		X		X			X

When the required address bits are present of the Address Bus, the data from the selected memory area is read onto the Data Bus when the Chip Select signal is recieved from the ROM/PROM Decoder.

A plug-in Add-On PROM board is available as an option. This add-on can have up to four IC's mounted on its PCB. The plug-in has option patches for several types of IC's. The patching pattern is the same as that on the main board. Capacitors for power source by-passing are included. Connectors at each end of the PCB mate with the two J9 connectors on the Digital Module. Note that the terminal numbers of the add-on connectors must match those on the main board. Note also that power should be OFF when mating the plug-in with the main board.

The add-on board receives up to 12 address bits from the Address Bus. Its 8-bit output is connected to the System Data Bus. Chip Select is determined by the ROM/PROM Decoder (UB3) on the Digital Module.

The CRT Refresh RAM (UD4-UD11) is similar in many respects to the user RAM. It has connections directly to the Data Bus for data to be written into memory. Output data from memory can be passed to the Data Bus through 81LS95 Tri-State Octal Buffer UE7 when gated on by lows at its terminals 1 and 19. The output data from the CRT Refresh RAM is connected directly to two 74LS377 latches, Character Latch UE6 and Status Latch UE5.

The row and column 6-bit addresses come from 74LS153 Multiplexers UE8, UE9 and UE12. The address sources include bits A0-A11 from the Address Bus -- used when the CPU addresses CRT Refresh RAM -- and six character counter outputs and five data row counter outputs from the 5027 CRT Controller, plus an output of CRT Timing PROM UG8 -- used when the CRT Controller addresses Refresh RAM. The Select signals for the Multiplexer originate in the CPU & Horizontal Decoder PROM UF8 and the CRT Refresh RAM Timing Multiplexer UG6. The four-line-to-one-line multiplexer chips each have two select lines. One select line is used to pass addresses from either the CPU (for new data input) or the CRT Controller (for recirculation of stored data). The other select line is used for passing row address and column address in sequence. No separate refresh circuitry is needed -- normal use provides frequent refresh.

The CRT Refresh RAM. treated as part of the microcomputer, is also very much associated with the display generator, the description of which follows.

Display Generator

The 5027 CRT Controller (UF9)*, under control of the microcomputer, generates CRT frame formatting signals such as horizontal and vertical sync, characters per data row, data rows per frame, row select data, blanking, and cursor video data. In some types of IC's the parameters are loaded into the chip from UA1 at power-up; in other types the parameters are fixed (masked). (See Appendix C for details of the 5027 CRT Controller unit.)

The microcomputer exercises control through a series of 8-bit words on the Data Bus and 4-bit register addresses on the Address Bus. The Chip Select signal is received from the System Decoder UF3. Data Strobe, which strobes D0-D7 data into the appropriate 5027 register, is the I/OW signal from the 8228 Bus Driver/Controller. The other input to the 5027, Dot Counter Carry, is from the 1.4976 MHz. output of Dot Counter UG7.

Character Counter and Data Row Counter Outputs from the CRT Controller go to the 74LS153 Multiplexers to become part of the address to Refresh RAM. Other outputs of the 5027 are used in generation of synchronizing signals for the Analog Board and in the addressing of PROMs in other parts of the display generator. These are discussed later in this section.

* The 5048 CRT Controller is similar and can be synchronized to the power line frequency by a jumper at pin 10.

Several PROMs of various types are used in display generation. The uses of these PROMs are taken up next.

The 82S123 CRT Timing UG8 is a 32x8 PROM whose outputs from memory provide timing signals for a number of devices in display generator circuits. One of its five address bits (A4) is the H6 Character Counter output from the 5027 CRT Controller. The other four address bits come from the 74LS163 Synchronous Binary Counter UG7.

The input Clock for that Counter is the 17.9712 MHz. Oscillator Signal. With the feedback from the D5 output of the CRT Timing PROM to terminal 1 of the Counter, the output at terminal 11 of the Counter is 17.9712 MHz. divided by 12, or 1.4976 MHz. (the character timing frequency, with a period of 667 ns.).

The 8-bit output from the UG8 memory is used as follows:

D0-D2	Clock inputs to Status, Color and Character latches UE5,UE4 and UE6. D1 is also the Shift/Load input to Shift Register UF5.
D3&D7	Inputs to CRT Refresh Timing Multiplexer UG6.
D4	Clock input to flip-flop in UG3.
D5	Clear input to Dot Counter UG7.
D6	One address bit to CRT Refresh RAM through Multiplexer UD12.

The 825131 CPU and Horizontal Decoder UF8 is a 512x4 PROM. Five bits of its 9-bit address are the H2-H6 Character Counter Outputs from the 5027 CRT Controller. One bit is the 5027 Chip Select from the System Decoder. Another bit is the A12 bit from the Address Bus (designating priority of access to the CRT Refresh RAM -- a low gives immediate access). Another bit is from a flip-flop in UG3. The remaining bit is the NAND of MR and MW.

The 4-bit output from memory is used for:

D0	RDYIN signal to Clock Generator UB1 via an AND gate.
D1	Power Supply Sync to the Analog Board.
D2	Timing trigger for the horizontal Drive circuit.
D3	Input signals to a flip-flop in UG3.

The 74LS74 Flip-Flop UG3's terminal 9 output, as a select A control for the CRT Refresh RAM address multiplexers (74S153 terminal 14). determines whether the 5027 or the 8080 addresses Refresh RAM. As the Select Signal to Multiplexer UG6 it causes UG6 to pass the appropriate set of inputs MW. RAS, CS, and CAS to Refresh RAM. ("A" inputs when the 5027 is addressing Refresh RAM and "B" inputs when the 8080 is addressing it.) Terminal 9 is low to select 5027 addresses and associated control signals for CRT Refresh RAM. It is high to select 8080 addresses and controls.

The 74LS157 Multiplexer UG6 has two sets of four inputs, one of which is gated to the four outputs by UG3.

INPUT TERM	SET	SIGNAL SOURCE	OUTPUT TERM	SIGNAL USE
2	A	+5V	4	One gate for Buffer UE7
3	B	MR from 74S438		(low is half of enable)
5	A	D7 from UG8	7	B Select to CRT Refresh
6	B	WR from 8080 or MR via gates in UF2 & UF4		RAM address multiplexers and CAS to Refresh RAM
11	A	+5V	9	MW for CRT Refresh RAM
10	B	MW from 74S438		
14	A	D3 from UG8	12	RAS and CS for CRT
13	B	WR or MR via UF2 & UF4		Refresh RAM

The 81LS95 Octal Buffer UE7 passes the CRT Refresh RAM output to the Systems DAta Bus only when the 8080 CPU Addresses Refresh RAM.

The components in the upper right portion of Schematic 100961 are associated with the character generation. Each character is defined in a 6x8 matrix, eight scan lines six dots long. Two 8-bit words are required for each character to be displayed. The first word is the "X" address to the Character Generator, which provides the dot pattern. The second word includes foreground color, background color and foreground blink status. These words are stored in the CRT Refresh RAM (32 lines x 64 characters x 2 words each = 4096 words).

The Character Generator UF6-UF7, two 1024 x 8 ROM's, provides storage for words describing 128 characters and a variety of graphics. It holds eight outputs for each character (one for each line of the character). These are accessed by a single "X" address (7 bits) for each character and by eight "Y" addresses (3 bits each). The "X" address is provided by the word from CRT Refresh RAM and the "Y" address is developed from the scan counts of the 5027 CRT Controller.

The 82S129 Scan Decoder UG9 is a 256x4 PROM that supplies the "Y" address inputs to the Character Generator with three of its outputs. (The fourth output is Cursor Infomation.) Its address bits include the 5027 CRT Controller's Scan Counter R0, Row Select R1 & R2, Data Row Counter DR and Cursor Video. It also receives the D7 bit of the first character word and a 1.875 Hz. signal from the Blink Counter.

The 74LS393 Blink Counter UG10 input is the 60 Hz. sync from the Analog Board through a Schmitt trigger in UE3. It divides this by 32 to yield the 1.875 Hz. blink rate. This is an input to two units in the generation of characters, cursor and graphics and to the 5501 Multifunction I/O Device (SENS, terminal 22). It is also used for the real time clock.

Three 74LS377 Octal Latches are involved in the processing of the information for characters. Each of these contains eight D-type flip-flops with common Enable and Clock inputs. In this case, with all three Enable inputs at Ground, information at the D inputs is transferred to the O outputs on the positive-going edge of the Clock pulse. The Clock pulses are generated by the CRT Timing PROM UG8. Output data from the CRT Refresh RAM is applied to the Character Latch UE6 input. The Character Latch output, together with the Scan Decoder UG9 and the R1-R2 outputs of the 5027 CRT Controller address the Character Generator UF6-UF7. An output of the Status Latch enables either UF6 (for characters) or UF7 (for graphics). The parallel 6-bit Character Generator output is changed to serial output by the 74LS166 Dot Shift Register and applied as one input to 82S131 Color PROM U7.

The other word for character generation is, immediately following the input to the Character Latch, addressed from CRT Refresh RAM to the Status Latch UE5. One output of the Status Latch determines which of the two chips of the Character Generator is enabled. Another output bit is applied with the 1.875 Hz. waveform to an AND gate whose output goes to the Color Latch. The other six Status Latch output bits (background and foreground color information) are addressed directly to the Color Latch.

The 74LS377 Color Latch is set by the seven input bits just described, plus and 8th bit from the Scan Decoder PROM UG9. Its output comprises eight bits of the 9-bit address required by the Color PROM UG5. (The 9th bit is the serial character data from the Dot Shift Register UF5.)

The 82S131 Color PROM UG5 is a 512x4 PROM. Three bits of its possible 4 bit output from memory are the Red, Blue, and Green signals to the Video Board. During sweep retrace the Blank pulse from the 5027 disables the Color PROM.

The 5027 CRT Controller generates synchronizing signals for the Analog Board to coordinate the sweep pattern with the video signals from the Color PROM. Two of these are supplied directly:

Horizontal Ramp Reset from H SYN, UF9 terminal 15.
Vertical Ramp Reset from V SYN, UF9 terminal 11.

The Horizontal Drive signal timing is determined by the D2 output of CPU & Horizontal Decoder UF8 and by monostable multivibrator UG4, both controlling a flip-flop in UG2 which actually generates the drive signal. When D2 goes low, the Horizontal Drive goes high as a result of this low at the terminal 4 Preset input to the flip-flop in UG2. When D2 goes from low to high, it starts the timing of the one-shot in UG4, which applies a high at the terminal 2 D input of the flip-flop in UG2. The high at UG2-4 causes the flip-flop to follow its D input on the positive-going transitions of the terminal 3 Clock input. So there is no immediate change in the Horizontal Drive signal -- it remains high. When the one-shot in UG4 times out (this time is adjustable by R20), the D input to the flip-flop goes low. Horizontal Drive goes low on the next positive-going Clock transition (the H0 Character Counter output of the 5027 CRT Controller). This is the Horizontal Drive signal used in the Analog Module.

This completes the circuit description of the Digital Module.

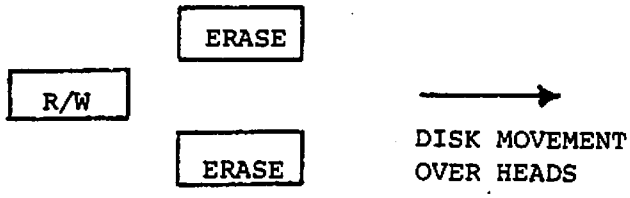
DISK DRIVE - 3621

The floppy Disk Drive uses the Standard 5 1/4" diskette package. Each of 40 tracks used for data (of 41 total tracks) is treated as consisting of 10 sectors with 128 bytes each -- about 1280 bytes per track, including formatting information, or 51,200 bytes per diskette. The home "zero" track (outer most track) is not used for data. The 3621 Intecolor has provision for use of two of these micro-disk drives. The basic unit includes one drive mounted in the right front of the cabinet. An optional external second disk drive can be connected in parallel with the Keyboard cable. Terminal configurations usually do not include a disk drive.

The rugged framework contains a DC drive motor which spins a diskette at approximately 300 RPM. A magnetic read/write head and an erase head are mounted on a slide mechanism which a 4-phase (or 3-phase) motor moves in and out across the recording tracks in 40 incremental steps. The Disk Controller Board, mounted on the disk drive framework, contains the record/reproduce amplifiers, drive motor speed control circuit, stepper motor drives, and control circuitry. The built-in disk drive is connected to the Digital Module by a flexible cable. Read and Write data are transferred to and from the Digital Module in serial form. Control data for the drive assembly is the 8-bit parallel output of the 5501 I/O Device (through an octal buffer) on the Digital Module. Bits 0-2 control the stepper motor, one of bits 4 or 5 controls the drive select , and bit 3 determines Write or Read. (Bits 6 and 7 are not used in the Disk Drive at present.)

The upper portion of Schematic Drawing 100873 shows the Reproduce Amplifier. Signals induced in the R/W Head by the diskette magnetic fields are connected through a filter and clipping circuit to one section of Dual Preamplifier UB2. Negative feedback is provided through R19 and amplifier phase compensation by R24-C4. The reproduce signal is carried through emitter-follower transistor Q1 and a noise reduction coupling circuit to the second section of UB2. (CR9 and CR10 block the center portion of the signal and most of the noise.) Negative feedback for the first section also is through a T-pad (R52, R53, C30). Section two has diodes CR3, CR4, CR7, and CR8 across R25 for output clipping. R27-C6 provide phase compensation. Operational amplifier UB3, functioning like a trigger, latches the signal to a section of inverting octal buffer UA2. The recorded signal effectively was only the transitions in the data. UB3 uses these to restore the data to original form at TP3. (The waveform at TP3 is inverted by UA2 and then inverted again by the line receiver in the Digital Module to be compatible with positive logic.)

Serial data to the Record Amplifier is passed through sections of inverting Octal Buffer UA2 to drive two transistors in Transistor Array UB1. When these transistors are enabled, their output drives the R/W Head to record data magnetically on the diskette. Current through the Erase Head keeps the width of the track within limits by erasing any portions that extend beyond the specified track width, (see sketch of head arrangement). Effectively, only the transitions are recorded. The original signal is recovered by the reproduce amplifier as described above.



HEAD ALIGNMENT

Control of the Record Amplifier is by bit 3 from the output of the Logic Board's 5501 I/O Controller. When WRITE is low (and the SELECT bit also low), it is passed through two sections of inverting Octal Buffer UA2 in series to be a low at UB1 terminal 12 and enable the Record Amplifier. (The low turns off transistor 14-12-13. The resulting high at term 4 turns on transistor 5-4-3 to pass the emitter current of the record amplifier transistors immediately above.)

The high at UA2-17, which is a result of a WRITE low, turns on a high-current Darlington in UA3 to pass current through the Erase Head to control the track record width.

The Disk Drive Motor speed is controlled by UA4 and associated circuitry. The transistor shown near the right edge of the UA4 block passes the drive motor current. The two transistors immediately to its left control its conduction. When the SELECT bit (bit 4 for the built-in disk drive or bit 5 for the optional added disk drive) is high, the 3-14 section of UA3 conducts to present a low at terminal 11 of UA4 and prevent current flow through the dirve motor. A SELECT low results in a high at terminal 11 to allow current flow through the motor. The output of the comparator in UA4 then controls the conduction of the control transistors. This is determined in part by the adjustment of R10 and in part of the output of the Pulse Generator. A tachometer attached to the drive motor (connected to UA4 terminals 3 & 4) and the pulse timing components R8-C2 control the Pulse Generator output.

If the drive motor speed becomes too high, the higher tachometer output operates through the Pulse Generator and comparator to reduce conduction through the control transistors and reduce motor current. Too slow a drive motor speed results in lower tachometer output, which serves to allow increased current through the drive motor. Disk drive speed is set for 300 RPM by adjustment of R10. If the motor should stall, the Stall Timer portion of UA4 prevents high motor current for any extended period of time.

The Stepper Motor moves the R/W Head and Erase Heads across the diskette one track at a time under control of bits 0-2. An appropriate bit combination results in a high out of the inverting Octal Buffer section in UA2 to turn on the associated Darlington in UA3. The 74LS138 at UA1 allows passage of only one low bit at a time to UA2.

The SELECT bit also is connected to the Octal Buffer gates (UA2 terminals 1 and 19). When the SELECT bit is high it gates all of the buffer sections into the high-impedance state to prevent passage of serial data in or out and operation of the stepper motor.

This gating also prevents flow of recording current. The SELECT high on the gate A of UA2 section 2-3, causes a high at terminal 12 of UB1. Transistor section 14-12-13 turns on to cause a low at terminal 4, turning off transistor section 5-4-3 to block emitter current from the record amplifier transistors above. Thus all functions of the disk drive assembly are disabled until a low SELECT bit commands the drive motor to start.

KEYBOARD

The 3600 Series Intecolor unit has a built in keyboard which may be one of three models. It is connected internally to Digital Module connector J1, accessible at the rear of the console. There are four parallel input lines and 12 parallel output lines, plus a CPU reset line, +5V and ground.

Schematic Drawing 100878 shows most of the Keyboard wiring as a matrix. The four input lines (connector terminals 3, 2, 5 and 4 in the upper left corner of the diagram) bring series of data bits O0-O3 from the Digital Module's 5501 I/O Controller periodically to the 74195 4-line-to-16-line Decoder in the Keyboard. The 74159 decodes the four binary bits into 16 mutally exclusive codes, 0-15, for the horizontal lines of the matrix. The seven vertical lines of the matrix are connected through 2,200-ohm resistors to +5V. Thus all seven matrix output lines (bottom of the schematic) are high except when key closure connects a low from the 74159 Decoder. This coded pattern is the input presented to the Digital Module.

The remaining five lines of the Keyboard's 12-line output (shown in the lower right portion of the drawing) also are connected to +5V through resistors. The five outputs are high except when the associated key is closed to give a low. The Reset key (drawing lower right) applies a low to the Logic Board's 8224 Clock Generator RESIN input. This results in a RESET to the 8080 CPU to force it back to an initial condition -- the CRT Operating mode.

An optional branched connector cable permits connection of an add-on Disk Drive as well as the Keyboard. Keyboard functions remain the same in this configuration.

NOTE: During the course of manufacture the keyboard was changed to provide two-key reset. The schematic for the current keyboard is drawing 101893. For the most part the theory of operation remains the same.

Addition of jumper W2 will allow single key reset — operation of the CPU RESET key alone. Without W2, one of the SHIFT keys or the COMMAND key must be held down while CPU RESET is pressed.

NOTE: Drawing 101815 now replaces 101354.

LOGIC MODULE - 3650/9650 SERIES

The Logic Module used in the 3650/9650 Series differs from that used in the other 3600 Series units. The three sheets of schematic drawing 101354 delineate the three major functions of the module:

Sheet 1	The microcomputer and most input/output circuitry
Sheet 2	The display generator
Sheet 3	The disk drive control circuitry and disk memory

This circuit description section will treat them in that order.

In the description following the term "high" refers to a voltage level of +5VDC and the term "low" refers to a level of zero volts (TTL positive logic).

Microcomputer

The heart of the microcomputer is essentially the four-chip set shown in the upper left portion of sheet 1 of drawing 101354 — UF4 (8080), UE4 (8224), UE3 (8238) and UF3 (5501).

The 8080 Central Processing Unit (UF4) is a general purpose microprocessor that can handle eight-bit words, has a repertoire of 78 instructions and can address up to 64K of memory. Appendix A at the rear of this manual describes the features of the 8080 CPU in some detail. Briefly, it requires power voltages or +5, -5 and +12 VDC and two timing signals Φ1 and Φ2. Other input control signals are Ready (RDY), Reset (RST), HOLD and Interrupt (INTR). There are output control lines for SYNC, Hold Acknowledge (HLDA), DBIN, Write ($\overline{WR}$) and WAIT.

All instructions and data in or out are handled by the eight-line data bus (DØ through D7). Connections of the various other devices to this data bus are, for the most part, through either the 8238 (UE3) or the 5501 (UF3).

The 16 address lines (AØ through A15) are buffered by UF5 and UF6 (f1LS95 Octal Buffers). The buffer chips are enabled by the normally low HLDA output of the 8080. When HLDA is high the buffers do not pass any address.

The 8224 Clock Generator (UE4) includes a 17.9712 MHz oscillator, controlled by crystal Y1. It generates two timing signals Φ1 and Φ2 at one-ninth the crystal frequency at an amplitude of 9 volts or more. These go directly to the 8080 CPU. There is also a Φ2 TTL level (5 volts) output and an output at the oscillator frequency. These latter two outputs are buffered by two sections of UE16 (74LSØ4 Hex Inverter).

When the Clock Generator receives a CPU Reset signal (a low) it generates the RST signal (active high) to reset the 8080. It processes the Ready In signal (active high) to produce the RDY signal (active high) for the CPU. It uses the SYNC signal, issued at the start of each machine cycle by the 8080 CPU, to generate a Status Strobe ($\overline{STSTRB}$) to indicate that the data bus has the status word describing the type of cycle in process.

The 8238 Bus Driver/Controller (UE3) has two major functions: It serves as a bidirectional driver for the data bus and it interprets the 8080's status word and control signals for other devices. As a bus driver it serves as a buffer between the 8080 CPU and many other devices in the Logic Module. As a controller it receives the status word (strobed in by the 8224's SSTSTB) and the $\overline{WR}$, HLDA and BUSBUF signals and interprets them to issue Input/Output Read and Write ($\overline{I/O\ R}$ and $\overline{I/O\ W}$), Memory Read and Write ($\overline{MR}$ and $\overline{MW}$) and Interrupt Acknowledge ($\overline{INTA}$) signals to other devices.

The BUSBUF input, in some applications simply the 8080's DBIN, is here generated by circuitry shown in the lower center portion of the schematic -- sections of UD2 (74LS74 Flip-flop), UD1 (74LSØ8 AND gate) and UA3 (74LS32 OR gate). One of the flip-flop's outputs (Q) is the enable for the 5501; the other output (pin 8) is first ANDed with DBIN (UD1 terminals 4-5-6) and the result ANDed with INTA. The D input of the flip-flop is high when UART (developed by PROM UA5 from address bits A12-A15) and either data bit D4 or D6 (indicating I/O read or write) are high. Otherwise the D input is low. The D input is clocked in on the positive-going transition of Ø2 when SYNC is high. When the 5501 is enabled, BUSBUF is low; it cannot return to high until the SYNC pulse during the first state of the next machine cycle. Also the 8080 must indicate by the DBIN signal high that it is in the input mode and there must be no Interrupt Acknowledge. This circuit, in a sense, provides a verified signal that the 8080 is ready to accept data through the 8238 Bus Driver/Controller.

The command from the 8238 to the memory to Write also has a form of verification. In two sections of UE18 (74LSØØ NAND gates, just below UE3 on the drawing) and a section of UE16 (74LSØ4 Inverter), the 8080's $\overline{WR}$ signal and the 8238's $\overline{MW}$ are used to produce the $\overline{VMW}$ (Valid Memory Write). Both $\overline{WR}$ and $\overline{MW}$ must be low in order for $\overline{VMW}$ to go low. This circuit enables use of either the 8228 or the 8238 Bus Driver/Controller.

While in this area of the drawing, note UE1 (74LS14 Schmitt Trigger Inverter), where the RST signal from the Clock Generator is inverted to become the $\overline{PCLR}$ signal (used in the Display Generator and Disk I/O).

The 5501 Multifunction Input/Output Device (UF3) provides interface between the keyboard and the RS-232C compatible serial I/O and the 8080 CPU. Interrupt signals also are processed through the 5501. Appendix B describes the 5501, outlining its various modes of operation. In this application, the enable signal (5501 EN) comes from the flip-flop in UD2 as described above. Timing signals Ø1, Ø2 and SYNC are received from the Clock Generator and the 8080 CPU. The CPU selects the mode of operation by the address combination of bits AØ through A3.

At intervals of 16,320 microseconds the 5501 generates an interrupt (through use of one of its timers) to cause the 8080 CPU to scan the keyboard for possible inputs. In these cases the parallel data from the 8080 is passed through the 5501 and UF2 (81LS95 Octal Buffer) to the keyboard. There are 12 lines of data from the keyboard. Eight of these are multiplexed by UF1 (74LS157 Quad Two-Line-to-One-Line Multiplexer) to four lines. These multiplexed lines and the other four make up the 8-bit response from the keyboard. The O7 bit from the 5501 (through UF2) is used for switching the multiplexer. A subroutine in software controls the scan and interprets the response.

While considering the keyboard, note that the CPU Reset ($\overline{\text{CPURST}}$) signal comes from the keyboard. When the keyboard's CPU RESET key is depressed, a ground is placed on pin 26 of J1 to apply a low to the Clock Generator's reset terminal 2. Reset at unit turn-on is provided by a delay circuit just above J1 on the drawing. Initially C52 has no charge, having been discharged through CR5 when the +5V supply went to zero at a previous system turn-off. Before the CPURST line can go high the +5V supply must first come up at turn-on. Then C52 must charge to some extent through R9 and CR6. This delay usually is sufficient to hold the CPURST line low until all power supplies are up enough to allow the CPU to operate correctly and be reset.

RS-232C Serial I/O is via the 5501 Multifunction I/O Device. The 5501 includes provision for converting the parallel data from the CPU to serial data for output and for converting input serial data into parallel data for input to the CPU. The 5501 EN signal and appropriate address bits select these modes of operation. Serial data from terminal 4Ø of UF3 for output goes to a section of UD4 (1488 Line Driver, bottom of schematic drawing), where it is inverted and output at RS-232C levels. (A logic "1" or "mark" is represented by -9 volts or more; a zero or "space" is represented by +9 volts or more at terminal 2 of J2.) This XMT signal is also routed to terminal 23 of the keyboard connector J1 if jumper W11 is in place. This provides for possible use in a micro-disk drive (not supported by standard 3650 Series software). Serial receive data (terminal 3 of J2) at RS-232C levels is inverted in a section of UE2 (1489 Line Receiver) and sent to the 5501 serial receive terminal 5 at TTL levels. Terminal 1 of keyboard connector J1 also is connected to the RS-232C receive at J2 terminal 3 if jumper W12 is in place. This allows for possible input from a micro-disk drive (not supported by standard 3650 Series software). The RS-232C signal for Data Terminal Ready is always high (+12V through R1) when power is on. Request to Send is under control of the D5 bit through the 5501, an inverter (UE1) and a gate (UD4). The Clear to Send is passed through sections of UE2 (1489 Line Receiver) and UE1 (74LS14 Schmitt Trigger Inverter) to parallel one of the keyboard outputs at terminal 1Ø of multiplexer UF1. In absence of a connection to the Clear to Send terminal 5 of J2, the point is pulled high through R7 to +12V. (Terminal 1Ø of UF1 is normally high unless pulled low by operation of the CAPS LOCK key on the keyboard or by a low at terminal 9 of J2.)

The 82S123 PROM UA5 was mentioned in connection with the generation of the 5501 ENable. This 32 x 8 PROM, near the middle of the schematic drawing, serves as an address decoder, using the higher order address bits A12 through A15 to generate a number of enable signals. For I/O addresses the upper eight bits of address duplicate the lower eight bits, making the address range ØØ to FF Hex. The I/O address map in the 3650/9650 Series is as follows (addresses not listed have not been assigned):

Address	I/O Device
ØØ - 1F	UF3 5501 Multifunction I/O Device
2Ø - 2F	UC3 1771 Floppy Disk Controller
5Ø - 5F	UA1 8304 T/R Enable (when TESTER is used)
6Ø - 7F	UA6 5048 CRT Controller
8Ø - BF	UA1 8304 T/R Enable (for normal X-Bus use)

UA5 also decodes two ranges of memory addresses to develop enable signals for the Screen Refresh RAM (SCRAM 7000-7FFF) and the Disk Buffer RAM (URAMS 6000-6FFF).

In the upper right portion of the drawing the X-Bus or Extension Bus is shown. The system driven data bus DB0-DB7 is connected through the 8304 Transceiver UA1 to XB0-XB7. UA1 normally is enabled by the X BUS signal from UA5. (When the Tester option -- jumper W3 instead of W2 -- is used, the TESTER signal from UA5 enables.) The T/R signal is developed in a section of UA3 (74LS32 OR gate) from the Bus Driver/Controller's I/O R and UA5's X BUS. When both signals are low the transceiver is put in the receive mode to transmit data from the X-Bus to the system driven data bus. Otherwise the chip is in the transmit mode to transmit data from the system data bus out to the X-Bus. When the Tester option is in use, the Bus Driver/Controller's MR signal is used to switch to the receive mode.

Also part of the X-Bus are the outputs of the 81LS95 Octal Buffer UA2. The chip is permanently enabled and passes address bits A0-A5 out to XA0-XA5. The XI/OR and XI/OW come through UA2 from OR gates in UA3. In each case an active low depends upon the X BUS (or TESTER) signal being low as well as the associated system I/O R or I/O W being low.

The remainder of Sheet 1 is associated with memory. The Read-Only Memory chips are shown as a block of four in the lower right area of the drawing. The eight outputs of each chip are connected to the system data bus DB0-DB7. The ROM outputs are high impedance except when a chip is addressed and enabled by a select signal. All four chips are addressed by bits A0-A9 directly and by bits A10-A12 via option fields at left and below the ROM block. (The option fields provide for use of a variety of ROM types.) The 12 bits give capability for 4k of address. Higher order address bits determine just which 4K. The address decoders for the ROM area of memory, 82S129 PROMs UF8 and UF7, are located just below UA5 on the schematic. UF8 uses address bits A8 through A15 to generate four Chip Select signals, one each for the ROM shown toward the right side of the drawing:

Address	Select Signal	ROM Chip
0000-0FFF	CS0	UF12
1000-1FFF	CS1	UF11
2000-2FFF	CS2	UF10
3000-3FFF	CS3	UF9

UF7 can be programmed to select four additional ROM when the add-on PROM board is connected to J8. The UF7 chip is part of the Add-on PROM option. Both UF8 and UF7 are enabled by the MR signal from the 8238 Bus Driver/Controller.

The User RAM UB9 through UB24 is shown in two blocks (above the ROM block on the drawing) of eight 16K x 1 chips each. A 32K unit has all 16 RAM chips. A 16K machine has only UB17 through UB24. These dynamic RAM chips require refresh at frequent intervals. The circuitry at left of the RAM blocks provide for refresh as well as for address multiplexing.

The 16K RAM chips require 14 bits of address AØ-A13. In order to conserve terminals on the chips, there is provision for address multiplexing to pass the address in as seven row address bits (strobed in by a Row Address Strobe) followed by seven column address bits (strobed in by a Column Address Strobe). The 3242 Address Multiplexer/Refresh Timer UA9 multiplexes address bits AØ-A13 in the required fashion, passing the row address through when terminal 3 (R/$\overline{C}$) is high and the column address when terminal 3 is low.

This control signal and two others associated with the generation of $\overline{RAS}$ and $\overline{CAS}$ are developed in the three flip-flops UE2ØA and B and UE21B just to the left of the 3242. In the absence of an address in either the User RAM range (8ØØØ-FFFF) or the Disk Buffer RAM range (6ØØØ-6FFF), the reset lines (terminals 1 or 13) of all three flip-flops are low. The URAS signal at UE2Ø pin 5 is low. As an input to a section of UE19 (74LSØ2 NOR gate, just left of the UB17-UB24 RAM block) it will not result in a low $\overline{URAS}$ signal to the RAM chips. The terminal 8 outputs of both UE2Ø and UE21 are high. The high from UE2Ø pin 8 conditions the 3242 multiplexer to pass a row address. The high UCAS from UE21 pin 8, as input to two sections of UE15 (74LS32 OR gates, near the lower RAM block on the drawing) causes both $\overline{UCASL}$ (Column Address Strobe for the lower 16K of RAM) and $\overline{UCASH}$ (CAS for the upper 16K of RAM) to be high.

A change occurs when the CPU addresses either the User RAM (8ØØØ-FFFF) or the Disk Buffer RAM (6ØØØ-6FFF) and either a $\overline{VMW}$ or $\overline{MR}$ is issued. The three flip-flops are released from reset when the terminal 1 output of NOR gate UE19 (just below UE21) goes high. This occurs only when both inputs are low. The $\overline{VMR}$ and $\overline{MR}$ signals are applied to one AND gate in UE17; when either of these goes low, the terminal 3 input of UE19 goes low. When the address is in the Disk Buffer range, the $\overline{URAMS}$ signal goes low (pin 2 input of AND gate UE17). When the address range is 8ØØØ or greater the A15 address bit is set. This bit is inverted in a section of UE16 to be the other input at terminal 1 of AND gate UE17). Thus when either A15 goes high or $\overline{URAMS}$ goes low, the pin 3 output of AND gate UE17 applies a low to the pin 2 input of NOR gate UE19. With both inputs then low, UE19 applies a high to the reset terminals of the three flip-flops to release them from the reset condition. On the next positive-going transition of the 17.9712 MHz CLK, the high at UE2Ø pin 2 is clocked through to make terminal 5 high. This high URAS, applied to NOR gate UE19 terminal 5 (over near the RAM block), results in a low $\overline{URAS}$ to all of the RAM chips. On the next positive-going transition of the CLK the URAS high is clocked into the next flip-flop (UE29 pin 12). The $\overline{Q}$ output of UE2Ø pin 8 goes low and this signal conditions the 3242 Multiplexer to be conditioned to pass the column address. Then on the next CLK positive-going transition the high from UE2Ø pin 9 is clocked into UE21 terminal 12; UE21's terminal 8 output goes low to produce a low $\overline{UCAS}$. This signal is applied to two OR gates in UE15 (terminals 9 and 5 in the gate sections near the RAM block). If the other input of either OR gate is low, a low $\overline{RAS}$ is applied to a RAM block. The $\overline{URAML}$ and $\overline{URAMH}$ signals determine whether a low $\overline{UCASL}$ goes to the lower 16K of User RAM or a low $\overline{UCASH}$ goes to the upper 16K. These two signals are developed in three sections of UA4 (74LSØØ NAND) near drawing bottom center. If both A14 and A15 are high, indicating address in the upper 16K of User RAM, they cause UA4 pin 3 to output a low $\overline{URAMH}$. If A14 is low and A15 is high, indicating address inthe lower 16K of User RAM, UA4 pin 11 outputs a low $\overline{URAML}$. These signals, applied with $\overline{UCAS}$ to the OR gates in

UE15, result in a Column Address Strobe to one of the two blocks of User RAM. At this time the User RAM outputs data onto the data bus DBØ-DB7 if the $\overline{VMW}$ signal is high. New data is written into User RAM from the data bus if the $\overline{VMW}$ signal is low. (The $\overline{VMW}$ signal is the Write Enable input at terminal 3 of the RAM chips.)

Refresh of the dynamic RAM chips is provided by the 3242 Multiplexer/Refresh Timer in conjunction with the three flip-flops in UE22A and B and UE21A and other circuitry. This refresh occurs at each 8080 CPU "instruction fetch" cycle when the CPU is not in a Wait or Hold state. It occurs at each Ø2 clock cycle when the CPU is in a Wait or Hold state. The 3242 has an internal counter which is used to provide what might be called 'dummy' row addresses during refresh. When this row address is output to the RAM chips, which occurs when the Refresh Enable terminal 2 of the 3242 goes high, and a Row Address Strobe is applied to RAM, all memory cells in the addressed row are refreshed. Their contents are unchanged. When the Count terminal 1 of the 3242 is switched to low, the internal counter is advanced to the next row address. Then if the 3242 pin 2 Refresh Enable is still high, a $\overline{RAS}$ refreshes the next row. In the section of UE17 just below the 3242, one input of the AND gate also is the Enable input to the 3242. When this input is high, refresh is enabled. The other input of the AND gate is the Ø2 clock inverted through a section of UE16. This signal, if UE17 pin 9 is high, causes the output at UE17 pin 8 to toggle back and forth between high and low with each Ø2 clock cycle. On the negative-going transition the internal counter in the 3242 is advanced. The positive portion, as an input to the NOR gate in UE19 just to the right, results in a low $\overline{URAS}$ for refresh of a row of memory cells.

If either the WAIT or HLDA signals, applied to UE19 terminals 8 and 9, goes high to indicate that the CPU is in a Wait or Hold state, the resulting low at UE19 pin 1Ø applied to the input of NAND gate UE 18 yields a high at UE17 pin 9 to initiate refresh. If the $\overline{REF}$ signal at the pin 9 input of UE18 goes low, refresh also is enabled. This $\overline{REF}$ signal is developed in the chain of three flip-flops UE22 and UE21A.

The resting state of the chain is with $\overline{REF}$ high. For when $\overline{REF}$ has gone low it resets the two flip-flops in UE22 to make the UE22 pin 9 and pin 5 outputs low. The low input to terminal 2 of UE21 is clocked in at the next positive-going transition of the Ø2 clock to make terminal 6 (the $\overline{Q}$ output) of UE21 high. This high, applied to the reset inputs of the UE22 flip-flops, releases them from the reset condition. An input can be clocked into UE22B (the M1 flip-flop) by the $\overline{STSTRB}$ as it returns high after indicating the first state of an "instruction fetch" cycle in the CPU. At this time the CPU's D5 bit was high to indicate instruction acquisition for the first byte. Pin 9 of UE22 then goes high. This high, input to the next flip-flop (T4), is clocked in by the $\overline{MR}$ signal as the read of an instruction from memory is completed and $\overline{MR}$ returns high. Pin 5 of UE22 goes high. This high, in turn, is clocked into the third flip-flop (REF) on the next positive-going transition of Ø2. This makes $\overline{REF}$ low to result in refresh of one row in each RAM chip. The low $\overline{REF}$ also resets the first two flip-flops in the chain. The resulting low at UE22 pin 5 is clocked into the REF flip-flop on the next cycle of Ø2 to make $\overline{REF}$ high again. The chain then awaits the next instruction fetch cycle.

Refresh also occurs at CPU Reset. The set signal for the REF flip-flop is the $\overline{\text{PCLR}}$, inverted from RST. RST goes positive at CPU Reset; $\overline{\text{PCLR}}$ goes low. The low sets the REF flip-flop to make its $\overline{Q}$ output at pin 6 low, resulting in refresh. $\overline{\text{PCLR}}$ is high except during CPU Reset.

One final comment on Sheet 1: Near the power input connector J6 at the top center of the drawing are a number of zener diodes. The nominal zener voltage of those across the 12-volt inputs is 15 volts; those across the 5-volt inputs have a nominal zener voltage of 6.2 volts. Under normal conditions with the power supplies in regulation, these diodes are floating across the inputs, drawing very little current. However, if power supply regulation is lost and the input voltages to this board increase, the zener diodes help to limit the rise to a value that will not damage the integrated circuit chips on the board.

Display Generator

The major components of the Display Generator section of the Logic Module, shown on Sheet 2 of Schematic Drawing 101354, are the Screen Memory (UB25 through UB32, drawing left center), the Display Generator chip (UE9, top right) and the CRT Controller chip (UA6, right center).

The Screen Memory is a 4096 x 8 Random Access Memory. Each of the eight 4027 chips (4096 x 1) stores one bit of the eight-bit word. For each character space on the CRT screen there are two words in memory, one to define the character and one to define the status (foreground color, background color, whether the foreground blinks and whether the character word is to be interpreted as a "character" or as a "plot block combination"). A total of 4096 words describes the CRT display (32 lines x 64 characters/line x 2 = 4096). The screen memory can be addressed by either the CPU or by the CRT Controller chip. The CPU addresses the memory to write in information to be displayed and for access to the memory for certain other purposes. The CRT Controller addresses the memory to route the memory words to the Display Generator chip for creation of the video signals.

Multiplexers UD6, UD7 and UD8 are dual 4-line-to-1-line multipexer chips which pass either the 12-bit addresses from the CPU (AØ through A11) or from the CRT Controller. A high on terminal 14 causes the CPU address to be passed; a low lets the CRT Controller access the screen memory. Each 12-bit address is transmitted as two 6-bit groups, the first as a row address and the second as a column address to the eight 4027 memory chips. The control signal at terminal 2 of the multiplexer chips is high to pass the row address, low to pass the column address.

The dynamic RAM screen memory requires refresh periodically (within 2 ms. intervals) to maintain the stored data. In this application the memory is read out in such a fashion that each row is accessed often enough for display to provide this refresh within the required interval; no other refresh provision is needed.

The screen memory is accessed by the CPU only during the horizontal retrace times. The CRT Controller has access during the scan to route the words describing the display to the Display Generator chip.

The CRT7005 Display Generator UE9 is an LSI circuit especially designed for this application. It includes Read-Only Memory which stores the data for 128 characters and 256 plot block combinations. Input address information from the Screen Memory and other sources results in output of three video signals in serial form for the red, green and blue video amplifiers.

Each character requires eight words in ROM, one for each CRT scan, a total of 1024 words for the 128 characters. Of the 10-bit address required for access to one of these words in memory, seven bits (SDØ-SD6) come from a word in screen memory (which effectively selects the character) and the other three bits (RØ-R2) come from the CRT Controller chip scan count (which defines the particular horizontal scan in process). The foreground color, background color and blink are defined by a second word from screen memory. The lower order three bits define foreground color; the next three

bits define background; the second most significant bit determines foreground blink.

The most significant bit of the status word, when set, defines the character word as the address for a plot block combination rather than for one of the 128 characters. In this case all eight bits of the character word are used as address to ROM and the remaining two bits needed for address come from the R1-R2 scan count bits. (Each character space is divided into eight plot blocks, so there can be 256 plot block combinations within a character space.)

The CRT Controller, with its Cursor Video (CRV) signal, alters the address to the Display Generator chip to cause the display of the cursor over whatever character or plot block is called for by the words in screen memory.

Other control circuits contribute to the Display Generator chip the Data/Attribute (D/A) signal to indicate which word is being presented from memory and an L/S signal to load and then strobe the appropriate word into latches within the Display Generator chip. There is a horizontal blanking signal (BLNK) during horizontal retrace and a vertical sync signal (V SYNC) from the CRT Controller for timing purposes. A low $\overline{\text{PCLR}}$ signal disables the video output whenever there is a CPU Reset.

The RTC output is a 1 Hz timing signal sent to the 5501 Multifunction I/O Device for incrementing the Real Time Clock display.

Certain optional connections are shown in a table at drawing upper right. Inputs to terminal 2 and 9 of UE9 are as shown (ground to 2 and +5V to 9) in the standard board. When the optional character board (which can provide alternate character sets such as Arabic) is in use the connections must be changed to make DDM (Direct Data Mode) terminal 2 +12V and terminal 9 -5V as indicated in the table. The input to terminal 27 is +5V when the power line frequency is 60 Hz and ground when 50 Hz.

Information describing the display has been presented to the Display Generator chip in parallel fashion; a six-bit word, for example defines which of the six dots in one scan of a character are foreground and which are background. For display this information must be output serially as the scan progresses across the CRT screen. The dot clock (VDC) input at terminal 12 clocks out the video at a rate consistent with the speed of the CRT horizontal scan.

The three color outputs determine the color of each dot as the scan progresses. These outputs of UE9 are buffered by sections of UE13 for transmission to the video amplifiers.

The 5048 CRT Controller UA6 also is an LSI circuit especially designed for this application. Its outputs include the Horizontal Sync and Vertical Sync for circuits in the Analog Module. The Vertical Sync is synchronized to the power line frequency by the L SYNC input from the Analog Module. When the chip is addressed by the CPU (A8-A11) for certain purposes (such as scroll, for example, or for load or read of the cursor location), a high CRTC signal indicates this fact; a low $\overline{\text{I/O OP}}$ signal strobes the data (DBØ-DB7) into or from the addressed register.

The Dot Counter Carry (DCC) input is a signal at the character rate frequency for timing. The chip outputs binary bits for the count of characters per line (HØ through H6), data rows (or lines) per frame (DRØ through DR4) and scans per character row (RØ, R1, R2).

Other CRT Controller chip outputs are the BLNK (blanking) high during horizontal retrace and the CRV (cursor video) high to define the cursor location.

The Horizontal Drive signal for the Analog Module is developed from the character count outputs HØ-H6. These bits plus two optional fixed bits constitute the address for the 82S131 PROM UA7 (in lower left quadrant of drawing). At given character counts the O1 and O2 outputs of UA7 go high to initiate the drive pulse; later these outputs go low to mark the end of the horizontal drive pulse. One of these outputs is used as the D input of HDRV flip-flop UD3; the input is clocked to the Q output by the character clock (DCC). Optional connections for the A7 and A8 input address bits of UA7 and to the O1-O2 outputs provide for timing adjustment to center the display on the CRT screen.

While considering UA7, note that another of its outputs O3 (P/S SYNC) is used for sync of the Analog Module's power supply switching rate to a multiple of the horizontal scan frequency. Four positive pulses per horizontal scan period are sent to the Analog Module via J5. The fourth output of UA7 (O4) is involved in control of CPU access to screen memory -- more on that in a moment.

Four outputs from the Display Generator section of the Logic Module to the Analog Module via J5 have now been mentioned -- Horizontal Sync, Vertical Sync, Horizontal Drive and Power Supply Sync. Near J5 at right center on the drawing, all of these have a measure of protection from spikes resulting from CRT arcs. There is a series 47-ohm resistor in each line and a zener diode to ground. The 5.1V diode prevents the line from going more than a fraction of a volt negative or more than about 5 volts positive.

Now back to the lower left portion of the drawing for development of the CPUGRT signal which limits access to screen memory by the CPU to horizontal retrace time. CPU address of screen memory is indicated by a low $\overline{\text{SCRAM}}$, input to two NOR gates in UE7. Memory Read is indicated by a low $\overline{\text{MR}}$ to one gate, Memory Write by a low $\overline{\text{VMW}}$ to the other gate. When both signals to one of the gates are low, a high is output to another NOR gate in UE7 (terminal 2 or 3). The output of that gate goes low; this negative-going transition is inverted to a positive-going transition in UE8 to clock the CPUQ flip-flop in UD5. Terminal 9 of UD5 then goes high and stays high until the flip-flop is reset. When CPUQ is high and CPUACC goes high to indicate that the horizontal retrace is in process, terminal 11 of UE5 applies a high D input to the CPUGRT flip-flop in UD3. This high is clocked through to the Q output of the flip-flop by the next positive-going transition of the character clock DCC. This high CPUGRT signal lasts one character time as the flip-flop's $\overline{Q}$ output at terminal 6 goes low to reset the CPUQ flip-flop in UD5 -- UD5's terminal 9 output goes back low to result in a low to the D input of the CPUGRT flip-flop, clocked through on the next DCC cycle.

Back at lower left on the drawing, the terminal 4 and 13 outputs of UE7 are also used as the SCWRT and SCRD signals elsewhere, the latter being inverted in a section of UE8.

The $\overline{\text{CPUWT}}$ signal circuit is in the same general area of the drawing. The $\overline{\text{I/O W}}$ and $\overline{\text{I/O R}}$ signals from the Bus Driver/Controller are applied to an AND gate in UE5. If either goes low, an $\overline{\text{I/O OP}}$ low is generated. Besides its use as a strobe for the CRT Controller chip, $\overline{\text{I/O OP}}$ is applied to another AND gate in UE5, terminal 4. The other input at pin 5 is from a NOR gate in UE7, high only when both CPUGRT and $\overline{\text{SCRAM}}$ are both low. Thus a low $\overline{\text{CPUWT}}$ results only from the combination of I/O R and I/O W high (for a high at UE5 pin 8) and CPUGRT and $\overline{\text{SCRAM}}$ low (for a high at UE7 pin 10). This combination gets a high at UE5 pin 6, which is inverted to a low at UE8 pin 8.

Remaining control signals are developed in the circuitry shown in the upper left quadrant of the drawing. The VDC flip-flop in UE6 uses feedback from its own $\overline{\text{Q}}$ output and the 17.9712 MHz CLK to toggle at the clock rate. This makes the UE6 pin 5 output a square wave at half the clock frequency. This approximately 9 MHz signal is the Dot Clock (VDC).

Other timing signals are developed by UE11 and UE12 (a 82S123 PROM and 74LS377 Latch at upper left). CPUGRT, SCWRT and three feedback outputs from UE12 constitute the address for the PROM UE11. The eight outputs of the PROM are the inputs to the Latch UE12, clocked in at the Dot Clock rate. The three outputs of UE12 PSØ, PS1 and PS2, fed back to UE11, result in a pattern of PROM outputs that repeat cyclically at one-sixth the Dot Clock rate. One of these feeds through UE12 to be the Character Clock DCC. Another is H/2, twice the character rate (or one-third the Dot Clock frequency). Two other outputs are the Row Address Strobe ($\overline{\text{SRAS}}$) and the Column Address Strobe ($\overline{\text{SCAS}}$) used to strobe addresses into the screen RAM (UB25-UB32). (There must be two of these during each character time to address the character and the status words in screen memory.) The final output, R/$\overline{\text{W}}$ for the screen memory, is high except when both SCWRT and CPUGRT are both high to indicate a CPU write into screen memory. Then R/$\overline{\text{W}}$ goes low.

The $\overline{\text{SRAS}}$ output of UE12 also is applied to the D input of the SMUX flip-flop in UE6. While SRAS is high, a high SMUX from UE6 pin 9 conditions the screen memory address multiplexers UD7-UD9 to pass the row address for the immediately following low $\overline{\text{SRAS}}$ to strobe in. Then SMUX goes low to cause the multiplexers to pass the column adress, strobed in by $\overline{\text{SCAS}}$.

The $\overline{\text{SCAS}}$ signal is inverted in a section of UE8 (just to the right of UE12) to provide the Load/Strobe for the Display Generator chip UE9. The PS1 output of UE12 and the VDC Dot Clock are used in a flip-flop in UD5 to generate the D/$\overline{\text{A}}$ signal by which the Display Generator chip distinguishes the character word from the status word.

The output of screen memory sometimes is put back on the system Data Bus. SDØ-SD7, in addition to addressing the Display Generator chip, are inputs to a 74LS374 Octal Latch UE1Ø. The words from screen memory are clocked into the latch by the H/2 signal. They are output to DBØ-DB7 when $\overline{\text{SCRD}}$ is low. Otherwise the latch outputs are high impedance.

Disk Drive Interface and Memory

The Disk I/O Control and Disk Memory circuits are shown on Sheet 3 of Schematic Drawing 101354. The principal chip, the FD1771 Floppy Disk Formatter/Controller, is shown at drawing top center. The Disk Buffer RAM is shown at drawing right. To the left of the RAM is an Address Decoder. A bit farther to the left, in drawing center, is disk hold circuitry. The bottom of the drawing has the drive selection circuits. The remainder of the drawing toward upper left is the data separator.

The FD1771 Floppy Disk Formatter/Controller UC3 is the principal interface between the microcomputer and the disk drive or drives. Its Data Access Lines (DALØ-DAL7) are connected to the system data bus via inverting buffers UC1 and UC2. UC1 is enabled for disk read operations and UC2 is enabled for disk write.

The Address Decoder PROM UE14, just below the data line buffers on the drawing, completes the address decoding for disk I/O. A decoder in the microcomputer (sheet 1) issues an FDC low when the I/O address is in the range of 2Ø-2F Hex. UE14 uses this signal and address bits A8-A11 to select the FD1771 and certain other circuits:

Address	Output
2Ø-27	1771EN
28	DRVSEL
29	RINT
2A	HLD

Back at the FD1771 chip, note that address bits AØ and A1 select internal registers when the chip is selected by $\overline{1771EN}$.

The $\overline{PCLR}$, issued when the microcomputer is reset, resets the FD1771.

$\overline{I/O\ R}$ and $\overline{I/O\ W}$, from the microcomputer's Bus Driver/Controller, determine whether the CPU access to the 1771 is read or write.

A square-wave clock is input at terminal 24, 1 MHz for use with 5.25" drives and 2 MHz for the 8" drives.

The Data Request (DRQ) output to the microcomputer indicates readiness for data input or output. The Interrupt Request (IRQ) is set at the completion of an operation, reset on loading of a neW command.

The chip has Direction (DIRC) and STEP outputs to control stepping of the disk drive record/reproduce head. The $\overline{WD}$ output is the serial data to be written in a write operation and Write Gate $\overline{WG}$ enables the write. A low $\overline{TRØØ}$ input from the drive indicates the drive head is over Track Ø. A low $\overline{WPRT}$ from the drive indicates Write Protect and terminates a write command. An $\overline{IP}$ low input from the disk indicates an index mark was encountered.

The ground at terminal 25 of the FD1771 conditions it for external data separation. The Separated Data and Separated Clock from disk read are input to the FD1771 at terminals 27 and 26.

The IRQ and DRQ are connected to an OR gate in UC11, which outputs a HLDCLR high when either IRQ or DRQ is high. The two signals also connect to gated buffers in UC4. The buffers are gated to pass the signals to two of the system data bus lines when both $\overline{\text{RINT}}$ (from decoder UE14) and $\overline{\text{I/O R}}$ (from the microcomputer) are low.

The Disk Hold flip-flop, part of UC9, is shown just below the FD1771. When its terminal 8 output is low, the gated buffer in UC4 passes its +5V input out as a high HOLD signal -- which goes back to the microcomputer. Normally the pin 8 output of the flip-flop is high. The $\overline{\text{PCLR}}$ associated with microcomputer reset works through a NAND gate in UC12, an OR gate in UE15 and an inverter in UC5 to reset the flip-flop's pin 8 output high. A high HLDCLR resets the flip-flop similarly. A HOLD can be generated during the first state of an 8080 machine cycle when data bit D4 or D6 is high to indicate address of an I/O device. A combination of a low $\overline{\text{HLD}}$ (from UE14) and the trailing edge of the $\overline{\text{STSTRB}}$ clocks the flip-flop to make the pin 8 output low and allow issue of a HOLD. The Disk Hold flip-flop can be reset to end the HOLD only by a HLDCLR (resulting from the FD1771's IRQ or DRQ high) or by CPU Reset (which gives a $\overline{\text{PCLR}}$).

Disk selection circuits, shown at the bottom of the schematic drawing, select the type and number of disk drive, the side of the disk and the clock frequency. The clock frequencies originate in a 16 MHz oscillator consisting of two inverters in UC18, crystal Y2 controlling the frequency. Binary counter UC19 serves as a frequency divider and outputs square wave clock frequencies of 4 MHz, 2 MHz and 1 MHz. These are fed to the inputs of UC17, a quad 2-line-to-1-line multiplexer 74LS157. The multiplexer outputs the MCLK, used in the data separator, and the CCLK, used by the FD1771. These are 2 MHz and 1 MHz respectively when 5.25" disks are in use and 4 MHz and 2 MHz when 8" disks are selected.

The disk drive select signals are issued by UC6, a 3-to-8 decoder 74S138. The A2 input determines whether the drive chosen is 8" or 5.25". The AØ and A1 inputs determine the number of the drive. Standard software supports four 8" drives and three 5.25" drives.

Flip-flops in UC7 and UC8 are involved in the selection process. When a drive selection is to be made, the microcomputer issues an I/O device address 28 Hex (decoded by UE14 to yield $\overline{\text{DRVSEL}}$) and an $\overline{\text{I/O W}}$. Appropriate bits are put on the data bus. When the $\overline{\text{I/O W}}$ or address is terminated, the data is clocked into the flip-flops. If DB5 is high, Disk Select flip-flop UC8 outputs a high at pin 5 and a low at pin 6. The high $5"/\overline{8"}$ output selects the 2MHz/1MHz clocks through multiplexer UC17. The low $\overline{5"EN}$ goes to decoder UC6 to select one of the MD drive select signals. Other data bits are clocked into four latches in UC7. DBØ and DB1 determine the drive number. DB2 selects disk side Ø or 1. DB3 can be used to disable all drive select signals by set of the UC6 decoder. (A high at terminal 5 of UC6 sets all outputs high.) Otherwise DB3 low enables the decoder to follow its inputs. DB3 low at this time, as an input to OR gate UC17, also allows the $\overline{5"EN}$ to determine whether the $\overline{\text{MOTOR}}$ signal is to be given to turn on the 5.25" drive motor(s). (8" drives do not require this signal.)

The external data separator, upper left on drawing, consists of a 74LS163 Binary Counter UC15, several flip-flops in UC8 and UC14 and a number of

gates. The read signals (FD DATA) coming from the disk drive include both data and clock pulses interlaced. (Data is recorded on the disk medium via an FM, or double-frequency, format.) These signals are sent into a chain of flip-flops and gates to become well-defined narrow pulses at one input to each of two AND gates in UC1Ø (terminals 2 and 12 of UC1Ø). These pulses are delivered to the gates by one of the flip-flops in UC14 (terminals 1Ø, 12, 9). This flip-flop's D input at pin 12 also is used through an inverter in UC18 (pins 5 and 6) to control loading of the binary counter UC15. The counter's clock goes through about 16 cycles during the interval between clock pulses in the FD DATA stream. If there is a data bit (representing a 1) between clock pulses in the stream, there are a nominal 8 MCLK cycles from the FD DATA stream's clock pulse to data pulse. The result of the timing is to cause the QD output of the counter, applied to one of the UC1Ø gates directly and to the other through an inverter, to allow only one of the gates to pass a pulse from the FD DATA stream. So one gate outputs the Separated Data (SPDATA) and the other the Separated Clock (SPCLK). The separated signals are sent to the FD1771 chip, which assembles the serial data into parallel data for output to the system data bus.

The 4K x 8 RAM Disk Buffer is shown on the right side of the schematic drawing. It consists of eight 4027 dynamic RAM chips. The multiplexed address (MUAØ-MUA5), row address strobe ($\overline{\text{URAS}}$), column address strobe ($\overline{\text{UCAS}}$), chip select ($\overline{\text{URAMS}}$) and write enable ($\overline{\text{VMW}}$) come from the same circuit area that serves the user RAM (see sheet 1 of the drawing). The RAM data inputs are connected directly to the system data bus. When the contents of the memory are to be read onto the data bus, the combination of $\overline{\text{URAMS}}$ and $\overline{\text{MR}}$ through the OR gate in UA3 enable Octal Buffer UA8 to pass the data.

This completes the description of the Logic Module. The circuits have been treated as three main divisions, as shown on the three sheets of the schematic drawing. However, all of the circuits are on the one printed circuit board whose layout is shown on Assembly Drawing 101356/357. Connections to other modules and to peripherals are as follows.

Accessible from rear of console when board is in place:

J1	Keyboard Connector	26-pin edge type
J2	RS-232C Connector	25-pin D-type
J3	X-Bus Connector	50-pin edge type

Internal, within the console:

J4	Video Connector	6-pin header/plug
J5	Sync Connector	6-pin header/plug
J6	Power Connector	8-pin header/plug
J7	Disk I/O Connector	34-pin vertical type
J8	Add-on ROM	Two 14-pin sockets

The Disk I/O Connector is connected by flexible ribbon cable to the built-in 5.25" disk drive (when present) and to a small PCB which terminates in the 34-pin EXT DISK edge connector, accessible from the rear of the console.

LOGIC MODULE FOR THE 3650 SERIES WITH IMAGE RESOURCE CAMERA

The 3650 Logic Module PCB was modified in early 1981 to provide space for two buffer ICs and a connector. A new schematic drawing number was assigned at the time.

Schematic 101815, a 3-sheet drawing, is the same as 101354 in most respects. Sheet 2 of 101815 shows the added components in the upper right portion of the drawing. Gated buffers UD9 and UD10 provide output of the horizontal and vertical sync signals along with the three color video signals. The buffer enables are under the control of the external device connected to J2.

All units in the 3650 Series use this newer PCB. Where the Image Resource interface is not required, the two ICs and the connector are omitted.

LOGIC MODULE — 3601 TERMINAL

Terminal versions of the 3600 Series use modified versions of the logic module of the microcomputer versions. The cost of the module is reduced by the elimination of the disk control and user RAM features.

Schematic drawing 101943, a 2-sheet drawing, shows the circuits of the current 3601 Logic Module.

Sheet 1 of 101943 is very similar to sheet 1 of 101815 for the 3650 Series Logic Module. One block of user RAM is replaced by a connector J8 for "Add on RAM". The X-bus feature is gone. Address decoder UE1 of 101943 differs from UA5 on 101815. Otherwise, the principal difference between the drawings lies in component nomenclature.

In like manner, sheet 2 of 101943 resembles sheet 2 of 101815. The provision for Image Resource interface (output of video signals and sync to an external device) is gone. Component designations vary, but circuit operation is much the same.

The 3601 Terminal needs no provision for disk drive control, so the circuits shown on sheet 3 of 101815 are not required.

Earlier manufacture 3601 Terminals used a stripped down version of the 3621 Logic Module. Schematic drawing 101278 is similar to 100961 in most respects except in the area of user RAM. There is no need for the address multiplexer. 128 bytes of static RAM scratch pad are in a single IC on a small add-on board (schematic drawing 101043).

THE REVISED 3650 ANALOG MODULE

Reliability was improved by a change in the analog module in later production units in the 3600 Series. At the same time a change to the pre-converged in-line CRT made alignment much simpler.

Analog Module Schematic 102350 shows the circuits for the unit's low voltage and high voltage power supplies and the circuits which produce the CRT's deflection signals.

This analog board, as noted in the drawing title block, is used in 2400 and 3810 Series terminals as well as in the 3600 Series terminals and desktop computers. Note Table 1 at drawing upper right which has the descriptions for those components peculiar to the 3600 version of the circuit. Differences are due mostly to the different horizontal deflection frequencies used.

AC Line Connections

The 3600 Series unit is equipped with a detachable three-conductor AC line cord. When the cord is properly connected to a grounded outlet, the unit chassis is always at earth ground potential.

The unit is designed to draw power from either 115V/50-60Hz or 230V/50-60Hz single-phase AC lines. Only single-phase lines, in which one current-carrying conductor is neutral or at earth ground potential, should be used. Two-phase lines such as are commonly found in 230V installations in the U.S. (both current carrying conductors "hot" with respect to earth ground) should not be used, because only one conductor is switched and fused in the 3600 Series unit.

AC is brought into the Analog from the line by way of J1 (at lower left on schematic drawing) on the unit's rear panel. It is routed through the line filter FL1, the main power switch SW1, the line fuse F1, and the line voltage selector switch SW2 to the the power supplies and the CRT degaussing circuit.

The setting of SW2 is very important.

The standard 3600 has SW2 set at the factory for 115V operation.
The line fuse F1 is type 3AG 1.5A/250V "Slo-Blo".

With Option 11, SW2 is set at the factory for 230V operation.
The line fuse F1 is type 3AG .75A/250V "Slo-Blo".

WARNING! Operation with SW2 in the wrong position for the power voltage applied can result in severe damage to the unit.

The CRT Degaussing Circuit

The degaussing circuit consists of a coil of wire placed around the CRT just behind the screen, a thermistor having a positive temperature coefficient, and a section of SW2.

The coil is connected in series with the thermistor (or posistor) selected by SW2 to the AC line -- R42 for 115V operation or R114 for 230V. When voltage is present on the line the selected thermistor is initially cold and accordingly presents a small resistance, which allows a large current to flow through the coil. As the thermistor warms up, its resistance increases and the current through the coil gradually diminishes to near zero.

The effect of this current flow is an alternating magnetic field, symmetrical about the screen, which gradually diminishes as the unit warms up. This field neutralizes any fields residual on the screen which, if allowed to build up and remain, would distort the CRT display.

The 12 Volt Power Supply

The 12 volt supply consists of a small power transformer T1, rectifier BR2, regulators U1 and U2, and filter capacitors C6-C9. (These are shown above and to the right of SW1 and SW2 on the schematic.)

One section of SW2 selects the proper tap on the primary of T1 for either 115V or 230V operation. The secondary of T1 is center-tapped and functions as a phase splitter providing about 14V RMS with respect to ground to each side of BR2. BR2, a VM18, operates as a pair of full-wave rectifiers connected back-to-back to provide both positive and negative outputs.

The positive output is filtered by C8, which charges to about +18V. This voltage is applied both to Zener diode CR9, which belongs to the undervoltage protection circuit to be described later, and to U1, an LM7812 positive voltage regulator. The output of U1, +12V +/-4%, is given further filtering by C9.

The negative output of BR2 is filtered by C6, which charges to about -18V, and applied to U2, an LM7912 negative voltage regulator. U2's output at -12V +/-4% is further filtered by C7.

Ripple on the +12V and -12V outputs is negligible. The regulation provided by U1 and U2 is such that their output voltages will vary less than 1% from their nominal values for line voltage swings between 95V and 175V and load current swings between 5ma and 1A. Normally, the load current on each of the +12V and -12V lines does not exceed 200ma.

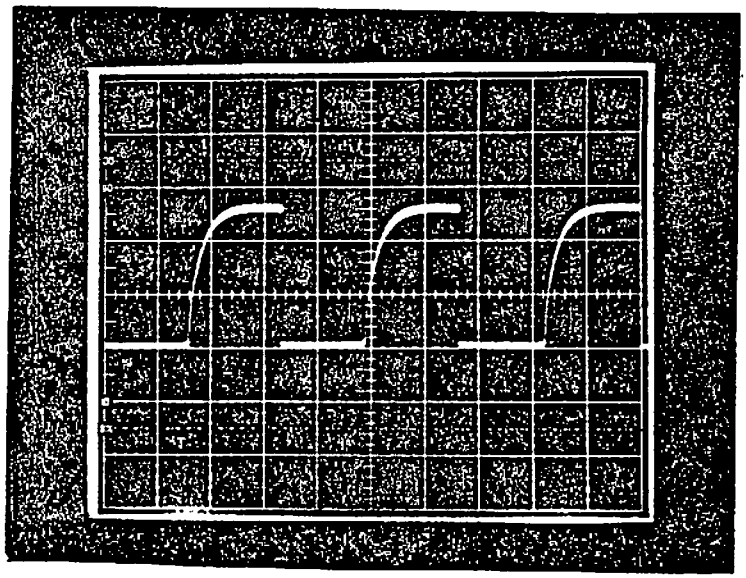
The Line Sync Generator

A line sync signal, which is utilized in the 3600's logic circuitry, is developed from the AC voltage present across one side of T1's secondary. The sync generator consists of diode CR15, transistor Q4, and their associated elements.

The sine wave voltage from T1 is applied to the cathode of CR15 and the base of Q4 through resistor R36. During the negative half-cycles of input voltage alternation, CR15 conducts and the base of Q4 is pulled nearly to ground. Q4 is therefore cut off, and its output is about equal to its collector supply voltage (+5V). When the input voltage becomes positive, CR15 stops conducting, and collector current begins to flow in Q4. This current flow is accompanied by a voltage drop across load resistor R38, which results in a drop in Q4's output voltage to nearly ground level.

The leading edge of the output signal is rounded somewhat by its use in the Logic Module. It consists of positive pulses having a frequency equal to that of the line voltage.

Oscilloscope
Sync - Line
Coupling - DC
Sweep - 5msec/div
Vert - 2V/div



The Switching Supply (+5V and +70V)

The main power supply in the 3600 furnishes up to 3A of current at +5V to the logic circuitry and sufficient current at +70V to operate the horizontal deflection and high voltage circuitry. Its size, weight and thermal dissipation are relatively low, both because power transfer takes place at a medium frequency (16kHz), which requires relatively small inductors, and because regulation is effected with pulse techniques rather than less efficient steady-state techniques.

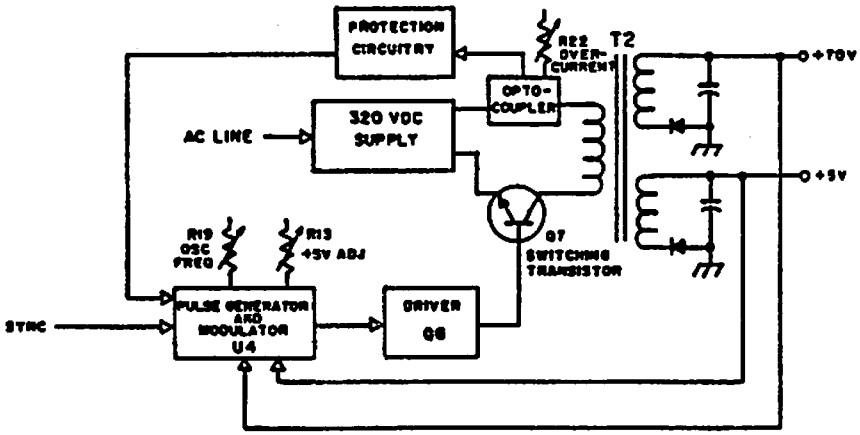
A rectifier circuit connected directly to the AC line furnishes about 320V DC to the primary of a power transformer. The primary current is switched on and off by a transistor, and energy is transfered to the secondaries following the "flyback" which occurs each time the current is interrupted. At these times current flows through the rectifier diodes in the secondary ciruits and the supply's reservoir capacitors are charged.

The switching transistor is made to function as a regulator by varying its duty cycle in accordance with changes in the loading of the supply. Load variations are reflected in instantaneous variations of the supply's output voltages. These voltages are fed back into the supply, where they are used to modulate the width of locally generated switching pulses. These variable width pulses drive the regulating transistor.

The switching pulses become wider as the supply's loading increases and its output voltage drops. The wider pulses allow greater amounts of energy to be transferred from the 320V supply to the transformer core. Consequently, more energy is released in the secondary circuits during the transistor's off times, current flow through the rectifier diodes increases and the reservoir capacitors are returned to the proper level of charge.

A simplified block diagram showing the functional relations of the major components of the supply is shown below — the switching signal generator and modulator, the switching transistor, the power transformer, the transformer's primary current source and the rectifiers and capacitors in the transformer's secondary circuits. Note also the overcurrent and undervoltage protection circuitry.

BLOCK DIAGRAM – +5V AND +70V SUPPLY



The functions of the various components of the supply will now be described in detail.

The source of DC voltage for the primary of the power transformer T2 is a supply consisting of rectifier BR1 and series filter capacitors C4 and C5.

In 115V operation BR1 is connected by one section of SW2 as a full-wave voltage doubler. When the line voltage swings positive, one arm of BR1 conducts and C5 is charged to about 160V. When the line voltage swings negative, the adjacent arm of BR1 conducts and C4 is charged to the same level. The output voltage is the sum of the charges on C4 and C5 or about 320V.

In 230V operation, SW2 connects BR1 as a full-wave bridge. During each half-cycle of line voltage alternation C4 and C5 are charged together to about 320V.

In both modes of operation the filter capacitors are charged through negative temperature coefficient thermistors R34 and R35. When the line voltage is first applied these thermistors are cold and present high resistances to the charging current. As the unit warms up their resistances decrease, allowing the capacitors to reach their full charge gradually.

This delaying function of the thermistors allows the power supply's overcurrent protection circuitry to become fully enabled before any appreciable current is available to a load.

Note that the +320V supply is not referenced to chassis ground. Any measurements in this part of the circuit must be made with ungrounded equipment.

> **WARNING!** When making measurements in this circuit, precautions against shock and damage to equipment must be taken because the +320V circuit common is floating — it may be "hot" with respect to ground. Because the +320V circuit common line is "floating" with respect to chassis ground, and because in 115V operation the "hot" side of the AC line is tied to the junction of C4 and C5, dangerous voltages may be present between 320-volt circuit common and earth ground.
>
> Use an ungrounded meter or oscilloscope, and avoid simultaneous contact with the 3810 chassis and the instrument cabinet while tests are being conducted.

The main primary of the power transformer T2 (drawing bottom center) is connected to the 320V DC souce in series with **regulating transistor Q7**, an MJ12005 power device.

When the switching signal at its base goes positive, Q7 turns on and and its collector-emitter voltage goes quite low. The resulting voltage across the primary of T2 causes current from the 320V source to build up in the winding. Energy is stored in the form of a magnetic field. The amount of energy stored varies with the on-time of Q7.

During this Q7 conduction time, voltages are induced on each of the secondary windings of the transformer (positive-going at pins 10 and 12) and on the auxiliary primary (negative-going at pin 5). These voltages reverse bias diodes CR11, CR12 and CR13 and no current flows either in the secondary circuits or in the auxiliary primary circuit.

When Q7's switching signal goes low, turning Q7 off, the main primary current is abruptly interrupted and a "flyback" occurs. Terminal 6 of T2 goes in a positive direction as a result of the voltage across it from self-induction. It reaches a peak of near +650V.

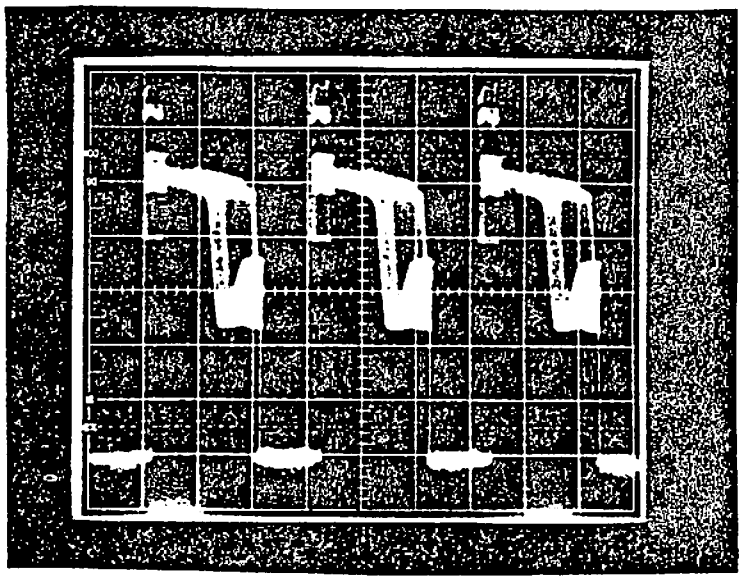
A "snubber network", composed by C19, CR18 and R24, limits the slope and magnitude of this flyback voltage pulse, thereby preventing damage to the switching transistor. In addition, a positive-going voltage is induced on the auxiliary primary winding at pin 5. This voltage rises no more than a diode drop above that of the primary supply voltage (+320V) — CR11 is forward biased at that point and prevents further rise. As CR11 conducts it stores additional energy in the magnetic field. This additional energy is somewhat proportional to the on-time of Q7 -- more on-time, more energy.

The primary flyback pulse induces voltages in the secondary windings of T2 at pins 10 and 12, forward biasing CR12 and CR13. Rectifier diodes CR12 and CR13 conduct, passing current created by the collapse of the transformer's field. The current flowing through CR12 and CR13 charges the reservoir capacitors C18 and C20 in the output section of the supply. The duration of conduction varies with the amount of additional energy stored in the primary windings and is roughly proportional to the previous on-time of Q7.

Following this conduction period, the voltages on the windings gradually return in irregular fashion to the levels they had at the beginning of the cycle.

In the voltage waveform at the collector of Q7 reproduced below, note that while the falling edges of the pulses — corresponding to Q7 turn-on — occur at regular times and are therefore sharply defined, the rising edges — corresponding to Q7 turn-off — start at different times and thus appear as blurry composites. (Note: The test oscilloscope is ungrounded, common lead of probe connected to T3 terminal 5.)

<u>Oscilloscope</u>
Sync - Int
Coupling - DC
Sweep - 20microsec/div
Vert - 100V/div
Trigger Slope - Neg

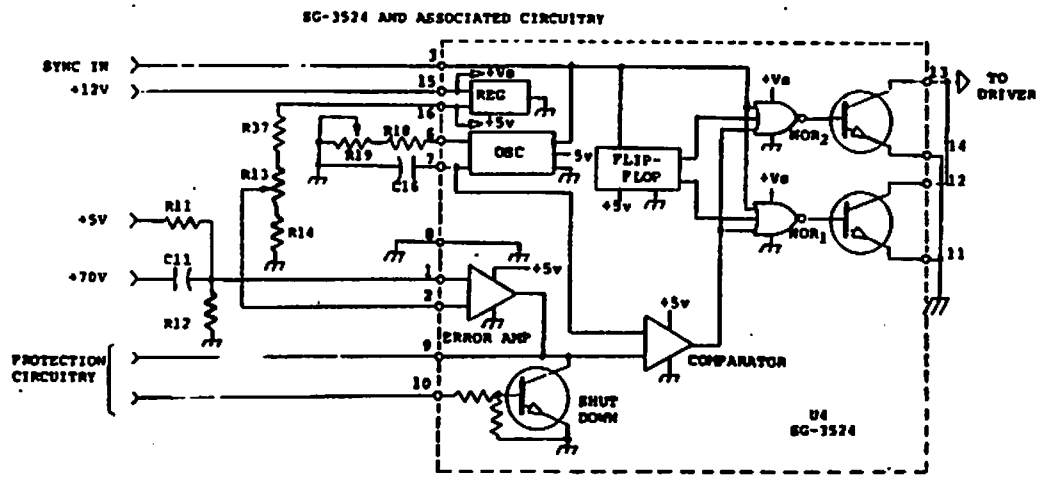


Because it is operated as a switch to create a flyback, Q7 is a very efficient regulator. Only the amount of electrical energy required to replenish the reservoir capacitors is drawn from the source. Relatively little energy is dissipated in the form of heat — as is the case in the steady state device (sometimes called a linear regulator, since the normal operating point is in the middle of the linear region of the current transfer or I_{be} - I_{ce} characteristic of the device).

Besides having greater efficiency than a steady-state regulator, a switching regulator is protected from short circuiting of the load. The transistor which bears the regulating function is not connected directly to the load and therefore is not subject to damage from instantaneous peaks of load current.

The regulator receives its switching signal from a transistor driver Q6, whose output is coupled to the base of Q7 via transformer T3. Q6 is driven in turn by a width modulated pulse generator. The operation of these components and of the control circuits associated with them will now be examined.

The switching signal is generated by U4 (drawing lower right), an SG-3524 integrated circuit, and associated circuit elements. A simplified block diagram of the SG-3524 is shown below.



U4 contains an oscillator which generates a signal having a linear sawtooth or "ramp" waveform. The frequency of the oscillator is determined by the time constant of external resistors R18 and R19 and external capacitor C16. R19 can be adjusted to give a frequency slightly below that of the horizontal sweep of the CRT, allowing the output of the oscillator to be synchronized with the sweep.

Synchronization does not play any role in voltage regulation within the supply. It is needed to prevent "jitter" at the edges of the CRT display which would otherwise result from the ripple on the +70V output to the horizontal and high voltage circuitry.

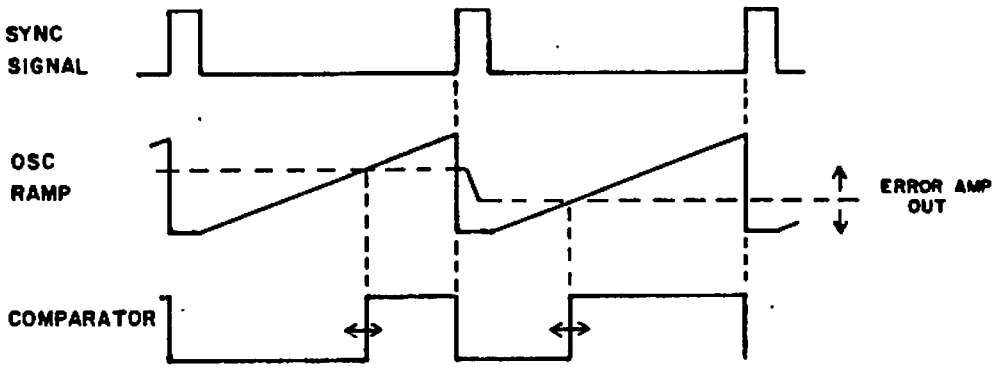
Synchronization is accomplished by applying a signal derived from the horizontal flyback transformer, FBT1, to the oscillator. A tap on the transformer provides a horizontal flyback pulse, which is used to turn on transistor Q5. (Diode CR16 eliminates any substantial negative swing.) Q5 functions as a Miller integrator, providing nearly rectangular positive output pulses.

These pulses are differentiated by C14 and the impedance of U4 at pin 3. CR17 eliminates the negative peaks. The positive peaks serve as sync signal to "pull" the oscillator up to the sweep frequency and hold its signal in a definite phase relation to the sweep. The trailing or falling edges of the sync pulses define the starting points of the oscillator's ramps, and the leading or rising edges of the pulses define the end points. The sync signal is also used to trigger a pair of flip-flops in U4 which have a role in forming U4's output pulses.

The sawtooth output of the oscillator is applied to one input of a comparator within U4. The other input of the comparator comes from an error amplifier, also within U4. The output of this amplifier is a function of the difference between a reference voltage at U4 pin 2, which is derived from a regulator within U4 and is adjusted by R13, and a voltage derived from the +5V and +70V outputs of the supply, applied to U4 pin 1. As this voltage drops, the output of the error amplifier rises. The error amplifier's output can vary between +.5V and +3.8V, following instantaneous changes in the sample voltage, which in turn follow changes in the supply's loading. With R13 adjusted to maintain the supply's output at +5V under normal loading, the reference voltage has a value at which its difference from the mean value of the sample voltage corresponds to about +2v output from the amplifier.

The error amplifier's output determines the level of a threshold, beyond which the oscillator ramp must rise in order to trigger a positive output from the comparator. When the error amplifier's output is +1V or lower, the comparator's threshold is zero, and its output goes positive as soon as the ramp begins. As the amplifier's output varies above +1V the comparator's threshold is raised and lowered with the rises and falls of this voltage, and since its output goes positive only after the ramp has reached this threshold the result is a series of pulses of varying widths. The on-time of switching transistor Q7 is proportional to the negative going portion of the comparator's output shown below.

PULSE WIDTH MODULATION BY THE SG-3524



The height to which the error amplifier can raise the comparator's threshold is limited by a network external to U4, consisting of resistor R8, Zener diode CR19, diode CR10, and capacitors C10 and C12. R8, CR19 and C10 provide a stable bias of +3V to the cathode of CR10. The anode of CR10 is tied to the output of the error amplifier. When this output is below +3V, CR10 does not conduct, and the signal passes to the comparator unmodified. When the amplifier's output rises above +3v, CR10 conducts, clipping the signal applied to the comparator.

This clipping circuit insures that the threshold of the comparator is never raised to the cutoff point (+3.5V), and consequently that a pulse is furnished by the comparator during every cycle of supply operation to turn off switching transistor Q7. If no pulse were furnished a switching signal would be produced which would overdrive the regulating transistor, possibly resulting in damage.

The comparator's output is further controlled by the undervoltage and overcurrent protection circuits. Both are capable of overriding the error amplifier and forcing the threshold of the comparator to zero, resulting in an output from the comparator sufficient to shut down the supply — that is, Q7 is not turned on.

The **undervoltage circuit is composed of Zener diode CR9, transistor Q3 and their associated elements. A positive voltage, furnished by BR2 and C8 in the 12V supply, is applied to the cathode of CR9. As long as this voltage remains above about +9V, CR9 conducts, current flows through resistors R5 and R6 and diode CR8, and a voltage is developed across R6 which biases Q3 on. When Q3 is conducting a current flows through collector load resistor R7 and the voltage at the collector drops to nearly ground potential.

Q3's collector is DC coupled to the base of a transistor within U4 (pin 1Ø). The collector of this transistor is in turn coupled to the output of the error amplifier. As long as Q3 remains on, the base of the transistor in U4 is low. It is therefore off, and has no effect on the error amplifier's signal to the comparator.

When the voltage on CR9 drops below +9V conduction ceases, and no positive bias is present at the base of Q3. Q3 therefore stops conducting, the voltage on its collector rises, and the transistor in U4 is turned on. When this occurs, its collector is pulled to ground potential and the output of the error amplifier is short-circuited. The error amplifier can no longer raise the threshold of the comparator, which goes to zero. The output transistors in U4 are not turned on. The voltage at U4 pins 12 and 13 remains high. No pulse to turn on switching transistor Q7 occurs.

Overcurrent control is effected by means of a 4N27 optocoupler, U3, linking the primary circuit of the power transformer to the control circuits. A voltage is developed across R23, in series with the primary of the power transformer, which is proportional to the current furnished by the supply. This voltage is adjusted by R22 and applied to the LED in the optocoupler. The illumination of the optocoupler's phototransistor varies with rises and falls of the load current, and the transistor's emitter-collector current varies accordingly.

If R22 is properly adjusted, the LED's illumination of the phototransistor becomes sufficient to cause Q2 to conduct when the current through R23 reaches a dangerously high value. When the phototransistor's illumination increases it becomes more conductive and the current through R1 and R4 increases. This increase in current is accompanied by an increase in the voltage across R4, and consequently in Q2's base-to-emitter voltage. When this voltage is sufficient, Q2 conducts, and its collector voltage drops to near ground level.

** NOTE: A later modification moved these sensing circuits to an added small PCB, which also contained a timing circuit for auto restart following a power interruption. See the description of this modification at the end of this analog circuit description.

With Q2 conducting, current flows through CR6, an LED which serves as an overcurrent indicator, and it is lighted. In addition, the cathode of CR7 is pulled to ground, CR7 conducts, pulling the anode of CR8 to ground, and Q3 is turned off. When Q3 is off, its collector voltage rises to about +12V and the shut-down transistor in U4 is turned on, disabling the error amplifier in U4. The comparator then produces a signal sufficient to shut down the supply.

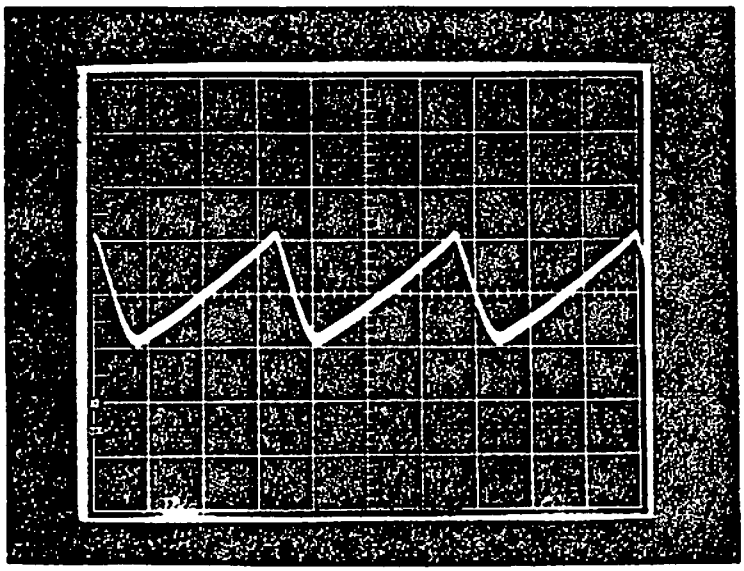
The comparator drives a pair of NOR gates within U4, and these gates in turn drive U4's output stage. These circuit elements utilize the signal from the comparator to produce the signal which appears at the output (pins 12 and 13 of U4). This signal consists of positive pulses having rising edges beginning at different times and falling edges which coincide with the falling edges of the oscillator sync signal. At Q6, the **driver transistor**, an NSD-U06, this signal is amplified and inverted, and the switching signal appears at the collector of Q6 as a series of positive pulses with regularly timed rising edges and irregularly timed falling edges. This signal is transformer coupled to the base of Q7.

The relation of the signals at succeeding stages of the generator is such that as the positive going signal from the comparator is made more narrow (in response to an instantaneous fall in the supply's output voltage) the positive going switching signal at the collector of Q6 becomes wider. A wider switching pulse results in a longer on time in the switching cycle of Q7. Since the amount of energy available to the supply's secondary circuits is directly proportional to this transistor's on time, more energy is released during the next off time, and the reservoir capacitors are recharged to the proper level. The diagram on the next page represents the signals at various stages within the supply and their interrelations.

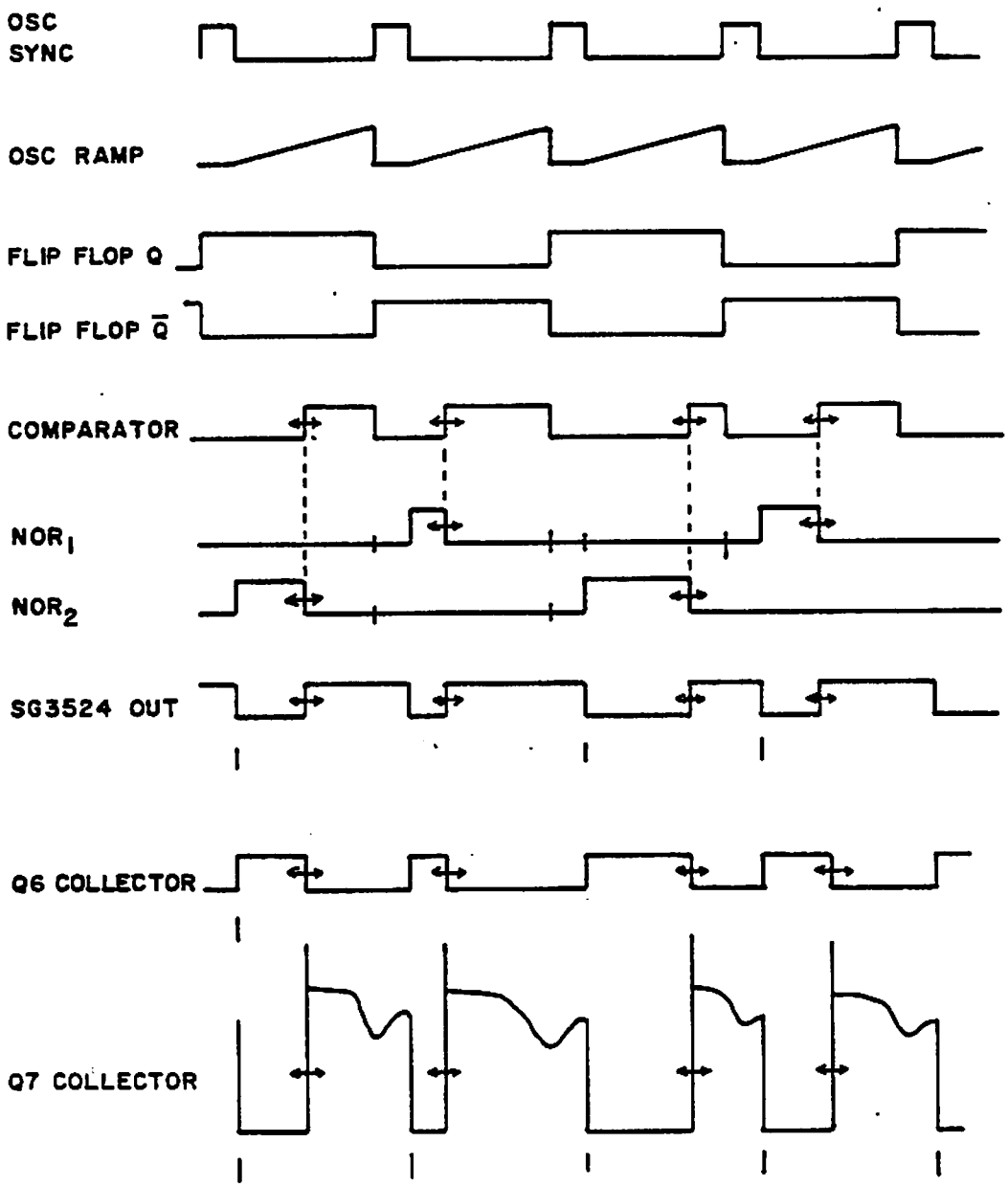
The regulation of the supply's 5V output is such that the voltage will vary no more than +/-2% with changes in loading. The 50/60 Hz ripple on the 5V output is typically about 0.1V peak-to-peak.

The 70V output should be within 10V of its nominal value when the 5V level is properly adjusted. The 50/60 Hz ripple on the 70V line is typically about 2V to 4V peak-to-peak. The oscilloscope photograph reproduced below shows the waveform of the ripple on this line.

<u>Oscilloscope</u>
Sync - Line
Coupling - AC
Sweep - 5 msec/div
Vert - 1 V/div



DEVELOPMENT OF SWITCHING PULSES
IN THE +5V AND +70V SUPPLY

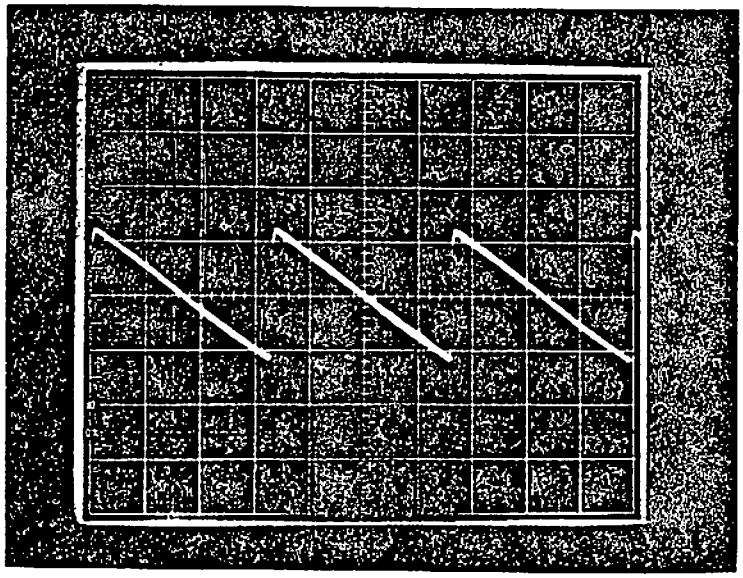


Vertical Deflection

Vertical deflection of the CRT beams is effected by means of a coil mounted on the neck of the tube and functioning as a magnet. A linearly decreasing current through the coil causes the beams to move at constant velocity from the top to the center of the screen. The current then increases linearly in the opposite direction, causing the beams to move from the center to the bottom of the screen. A sharp swing of the current from its peak negative value to its peak positive value then causes a rapid retrace of the beams to the top of the screen. The screen is swept vertically at 50/60 Hz (i.e., at the line frequency). Accordingly, the cycle period of the deflection coil current is either 20 or 16.67 milliseconds. Of this period, about 0.5 millisecond is devoted to retrace.

The oscilloscope photograph reproduced here shows the waveform of the vertical deflection signal. The oscilloscope was connected across R81 to obtain the trace. The voltage measurable at this point is proportional with and in phase with the current in the deflection coil.

Oscilloscope
Sync - Int
Coupling - DC
Sweep - 5 msec/div
Vert - 2 V/div

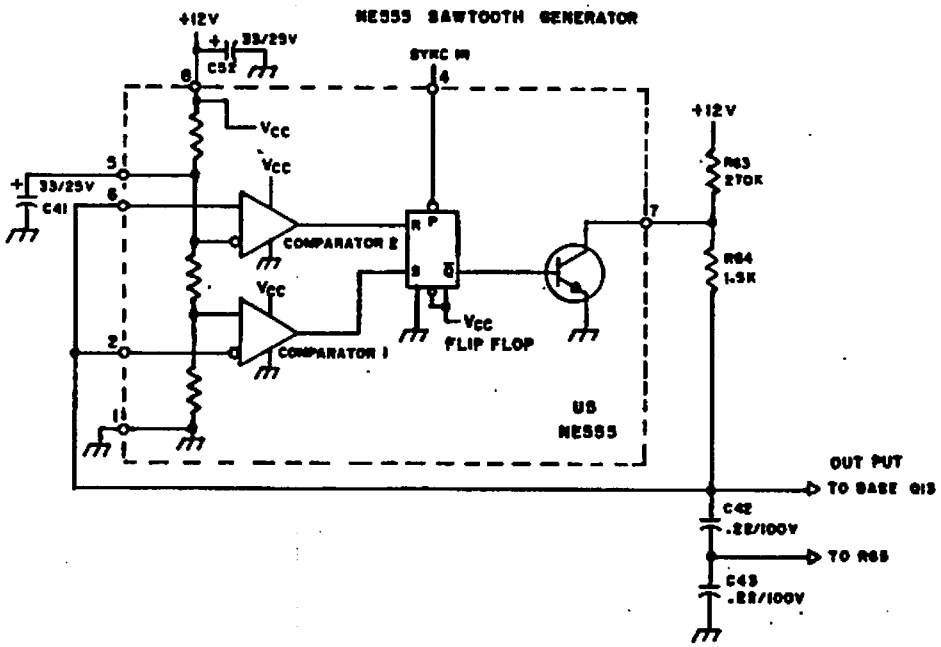


The vertical deflection circuitry, on the 3600's analog board, includes a linear sawtooth generator, a class AB power amplifier, a device for centering the vertical sweep, and a device which compensates for differences between the radius of curvature of the screen and the radius of the sweep ("pincushion" circuit).

The **sawtooth generator** is built around a Texas Instruments NE555 integrated circuit, U5. The NE555 monitors the voltage across series capacitors C42 and C43 and determines when they should be charged and discharged. When this voltage goes below about 1/3 of the supply voltage (+12V), the capacitors are allowed to charge from the supply through resistors R63 and R64. Because of the large value of R63, the time constant of this RC circuit is large with respect to the period of an operating cycle. Therefore the rate of change of the current in the capacitors (and of the voltage across them, which varies inversely with the current) is very nearly constant over this period, and a ramp waveform is produced.

When the voltage across C42 and C43 reaches 2/3 of the supply voltage, the NE555 pulls the junction of R63 and R64 to nearly ground level. At this point, the capacitors begin to discharge through R64. Since R64 has a relatively small value, the discharge is very rapid. The voltage across C42 and C43 falls quickly below 1/3 of the supply voltage, at which point the NE555 lifts the resistor junction above ground and charging begins again.

An understanding of the way the NE555 performs its function depends on a knowledge of the circuitry within it. This circuitry is included in the simplified diagram of the sawtooth generator given below. It is described in the paragraphs immediately following.



The NE555 contains two comparators, an RS type flip-flop, and a transistor. Reference voltages are supplied to the comparators from an internal voltage divider. Input voltages are supplied by C42 and C43. The first comparator sets the flip-flop when the voltage at its input, called the trigger input (at pin 2), falls below this comparator's reference voltage (1/3 the supply voltage). When the flip-flop is set, its inverted output signal is a logic low (i.e., near ground level). This low signal is applied to the base of the transistor within the NE555, preventing it from conducting. The voltage at the collector of this transistor, which is tied to pin 7 of the NE555, and by way of pin 7 to the junction of R63 and R64, is then dependent upon the drop across R63 which results from the charging current in the RC circuit described above.

The second comparator resets the flip-flop when the voltage at its input, called the threshold input (at pin 6), rises above that comparator's reference voltage (2/3 the supply voltage). When the flip-flop is reset, its inverted output signal is a logic high. A high signal from the flip-flop at the base of the transistor allows it to conduct. During conduction the junction of R63 and R64 is near ground, since the transistor's collector current causes a drop across R63.

It can now be seen that the frequency of the sawtooth generator's output depends on four parameters:

1) the time constant of C42 and C43 combined and R63 and R64 combined

2) the threshold level of the NE555's second comparator

3) the time constant of C42 and C43 combined and R64 alone

4) the trigger level of the NE555's first comparator

The first two parameters determine the slope and end point of the rising (voltage) ramp. The second two parameters determine the slope and end point of the falling part of the sawtooth, hence the beginning point of the ramp. Nevertheless, this is the case only when the generator is free-running. The application of a sync signal modifies the operation of the generator in a way described below.

Synchronization is necessary to insure that the vertical sweep starts slightly before video signals are applied to the CRT cathodes and that vertical retrace occurs while the screen is "blanked". A positive-going sync signal is supplied by the 3600 Logic Module. A 5048-type CRT Controller device, whose operation is synchronized to the power line frequency, provides the sync signal. It is routed to the vertical deflection circuitry by way of J5, pin 1, on the analog board. The signal, although labeled VSYNCBL, is a logic low (near zero voltage) during most of the sweep cycle period. It goes high (near +5V) for about 170 microseconds at the sweep rate.

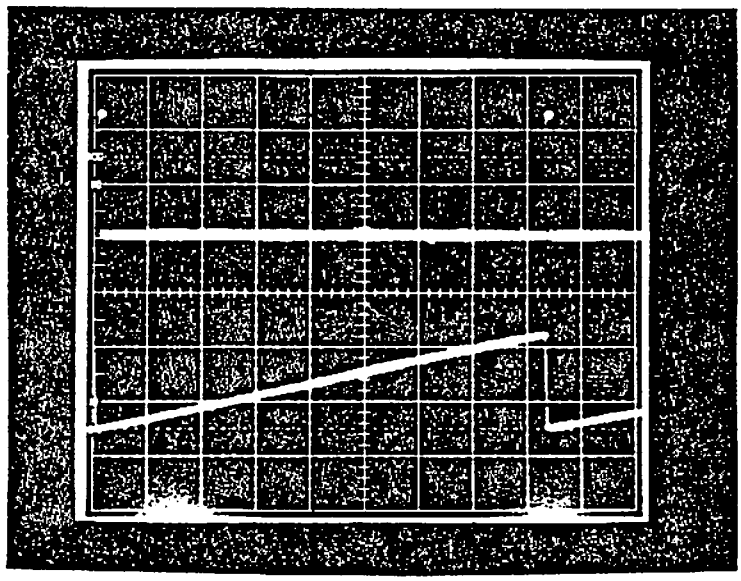
The VSYNCBL signal is applied to the emitter of Q11, a 2N4124 transistor, through a differentiating circuit consisting of C40, R60 and R61. (Note that the 3600 Series uses Q11 rather than Q12). Except when the sync signal goes high, Q11 has no forward bias. Consequently, the voltage at Q11's collector is about equal to the supply voltage. This voltage, applied to the preset terminal of the flip-flop within U5, allows the R and S inputs to the flip-flop to determine its output.

When the VSYNCBL signal goes high, a sharp positive-going voltage pulse, its shape resulting from the differentiation of the sync pulse, is applied to the base of Q11. The transistor's base-to-emitter voltage swings sufficiently positive to bring about conduction. As a result, there is a momentary voltage drop across Q11's collector load resistor, R62, and the preset terminal of the flip-flop in U5 is pulled nearly to ground. This low at the preset terminal overrides the R and S inputs and makes the inverted output of the flip-flop low. U5's transistor is accordingly cut off, the junction of R63 and R64 is lifted from ground, and C42 and C43 begin to recharge.

Proper synchronization requires that the generator's free-running frequency be somewhat lower than the frequency of the sync signal. This signal can then take over from the first comparator in U5 the function of determining the beginning points of the ramps. The effect of the sync signal's take-over is a rise in the generator's operating frequency and a decrease in the peak-to-peak amplitude of its output signal.

The rise of the VSYNCBL signal then coincides with the beginning of the ramp. This relationship is demonstrated in the oscilloscope photograph reproduced below. The VSYNCBL signal appears at the top; the sawtooth signal (taken from the emitter of Q13) appears at the bottom.

Oscilloscope
Sync - Int
Coupling - DC
Sweep - 2 msec/div
Vert - 2 V/div
(each channel)



The output of the sawtooth generator is applied to the base of Q13, an MPSA14 Darlington transistor which is connected as an emitter follower. Q13 provides buffering of the generator's output and impedance matching to the following amplifier. In addition, its emitter resistor, R68, provides a variable feedback signal to C42 and C43. R68 can be adjusted to smooth out any non-linearity in the ramp.

The class AB power amplifier consists of transistors Q14-Q17 and their associated circuit elements. At the input of the amplifier the driving signal is combined with AC and DC feedback signals. AC feedback is derived from C49 and R81 and routed to one end of the resistor chain consisting of R66, R67 and R69. The signal from Q13 is applied at the other end of this chain. A combination of the driving signal with AC feedback is taken from R67 and coupled to the base of Q14, an MPS-A05, through C44. The amplitude of this signal and hence the size of the vertical sweep can be varied by adjusting R67. DC feedback is applied to Q14's base through R71.

The amplifier's operating cycle begins as the ramp at Q14's base starts to rise. Q14's collector current is initially small and rises gradually with the ramp. This gradual increase of current, conducted by CR30 and CR31, is accompanied by an increasing voltage across R74 and R75, which makes the bias at the bases of transistors Q15 and Q16 less and less positive.

The first part of the amplifier's operating cycle corresponds to the first half of the ramp at Q14's base. During this period Q16 is on and Q15 off. Q16's conduction allows C49 to charge through the deflection coil. As this part of the cycle begins, CR32 is forward biased, because C48 and C49 have been discharged during the previous cycle while Q16's emitter has been pulled to a potential near that of the supply by the discharge of C46.

Q16 has remained saturated during the last part of the immediately preceding cycle, its base having been driven very positive as a result of the sharp fall of the sawtooth signal at Q14, and then heavily charged by the discharge of C46. When CR32 begins to conduct, the voltage at Q16's emitter immediately drops to about +30V. C46 therefore starts recharging. Since Q16's base is still saturated, the transistor can immediately begin to conduct the large current initially required for the linear charging of C49.

C49 and the deflection coil constitute a series LC circuit having a net capacitive reactance at the amplifier's operating frequency. It follows that the current in this circuit is initially large. As C49 charges, this circuit current, controlled by Q16, decreases linearly to zero.

The second part of the operating cycle begins when Q15 is turned on by the continuing increase in the voltage across R74 and R75. Q15 is conductive during the second half of the sawtooth generator's ramp. Its conduction begins a little before Q16 turns off. Its emitter current is supplied by the discharge of C49, through R78. The voltage drop across R78 keeps CR32 reverse biased during this part of the operating cycle. The current which begins to flow through Q15's collector resistor, R77, results in a voltage across this resistor which biases Q17 on. With CR32 biased off and Q17 able to conduct, C49 begins to discharge through the deflection coil and Q17. As current begins to build up linearly in the coil (flowing in a direction opposite that of the first part of the cycle), Q16 is shut off.

The third and fourth parts of the amplifier's operating cycle occur during the falling portion of the sawtooth signal applied at the base of Q14. As the voltage at the base of Q14 drops sharply, there is a rapid drop of Q14's collector current, accompanied by a sharp rise in the voltage at the base of Q15 and the base of Q16. Q15 is cut off by this change in base voltage, while Q16 is driven into saturation. The positive-going signal at Q16's base allows a large emitter-base current to flow. This current is supplied by the discharge of C46, and the base of Q16 is saturated. As a result, collector current continues to flow throughout the third and fourth parts of the cycle, allowing a smooth transition into the next cycle, when Q16 again controls the charging of C49. Meanwhile, as C46 discharges, Q16's emitter voltage is raised very nearly to the level of its collector supply (+45V).

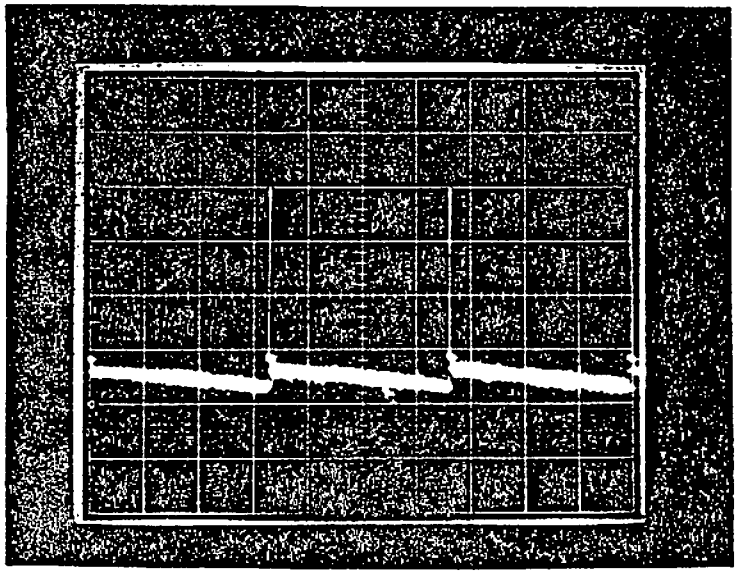
The third part of the cycle commences with the shut off of Q15. At this point, voltage at the base of Q17 falls and Q17 is turned off. The current in the deflection coil, which was increasing linearly as C49 discharged, now falls rapidly to zero. The steep current gradient in the coil is due to the fact that C48 is now included in the deflection coil circuit.

C48 was effectively shorted during the first two parts of the cycle. But when both Q16 and Q17 are off it functions in conjunction with C49 as part of a parallel LC circuit, which includes the deflection coil and R81. This circuit has a net inductive reactance at the operating frequency of the amplifier. Hence, a flyback occurs when Q17 is abruptly cut off. A voltage is induced across the deflection coil which allows C48 to charge to a very high value (about +175V) as the field around the coil collapses. While C48 absorbs the coil's energy, CR32 remains reverse biased. C47, connected across CR32, prevents damage to the diode by the high peaks of reverse voltage.

During the fourth part of the cycle, C48 discharges through the coil. The current in the coil, which fell rapidly to zero during the third part of the cycle, now builds up very rapidly in the opposite direction. As the voltage across C48 falls, CR32 is again forward biased. Therefore, oscillation cannot be sustained in the parallel LC circuit. Instead, as the deflection coil current reaches its peak value, a new operating cycle begins.

The oscilloscope photograph reproduced below shows the waveform of the voltage at the deflection coil (pin 1, J6). The sharp spikes represent the charging and discharging of C48 (flyback pulses).

<u>Oscilloscope</u>
Sync - Int
Coupling - DC
Sweep - 5 msec/div
Vert - 50V/div

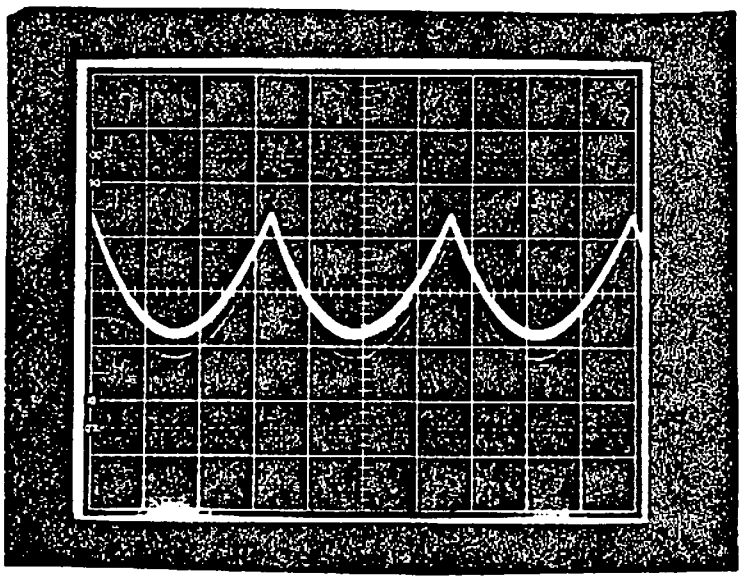


The circuit consisting of Q19 and its associated elements functions as an adjustable DC biasing device used for centering the vertical deflection coil. The bias level varies with the collector current of Q19, which is determined by the setting of R89.

A further circuit associated with the vertical amplifier, built around Q18, an MPSA14 Darlington transistor, has the function of generating a "pincushion" signal. This signal is developed from the vertical ramp and applied to the high voltage regulator. It makes the +60V used in the horizontal and high voltage circuits slightly lower at times corresponding to the beginning and end of the vertical sweep. This results in slightly smaller horizontal sweeps and lower CRT anode potentials at these points. Such decreases are necessary to maintain the width of the display constant throughout the vertical sweep, compensating for differences between the radius of curvature of the screen and the radius of the sweep.

The voltage across capacitor C49 has the shape of an inverted parabola. (C49 essentially functions as an integrator of the sawtooth vertical deflection signal.) This is coupled through C50 to the base of Q18. Q18 inverts the waveform and the vertical parabola, to be used for horizontal pincushion, appears at the collector of Q18. The oscilloscope photograph reproduced below shows this signal (taken from the collector of Q18).

<u>Oscilloscope</u>
Sync - Int
Coupling - AC
Sweep - 5 msec/div
Vert - .5V/div

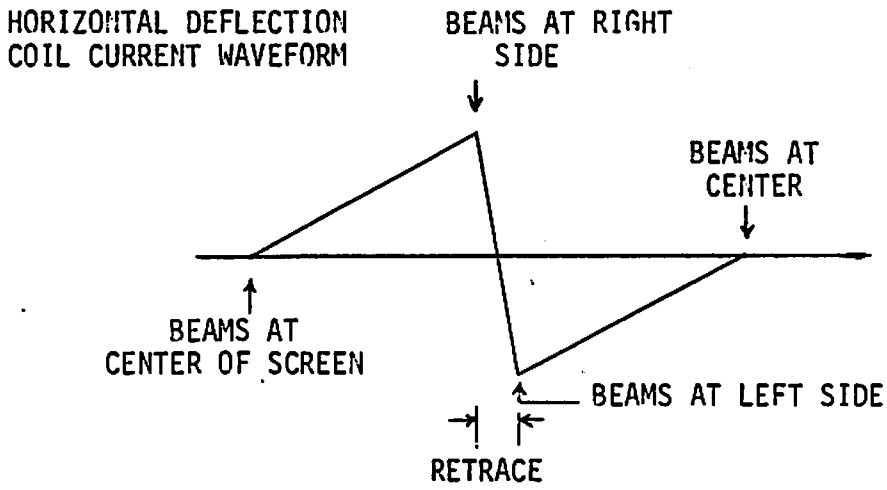


Potentiometer R84 is used to adjust the amount of this parabolic signal to be applied to the voltage regulator circuit through C74 and C68. R84 is adjusted for a display with straight sides. (See the Adjustment Procedure.)

Horizontal Deflection

Horizontal deflection of the CRT beams is effected by means of a coil positioned on the neck of the tube. An alternating current is made to flow in the coil, which then functions as a magnet. The current has a cycle period of about 63 microseconds, corresponding to a sweep rate of near 16KHz. At the beginning of a cycle, this current starts increasing linearly from zero to its peak positive value. As it does so, the beams are deflected from the center of the screen to the right side at a constant velocity.

The current then changes direction very quickly, going from its peak positive value to its peak negative value quite rapidly. Accordingly, a "retrace" occurs, in which the beams are moved very rapidly to the left side of the screen. At this point, the current begins decreasing linearly from its peak negative value back to zero, and the beams are returned to the center of the screen.

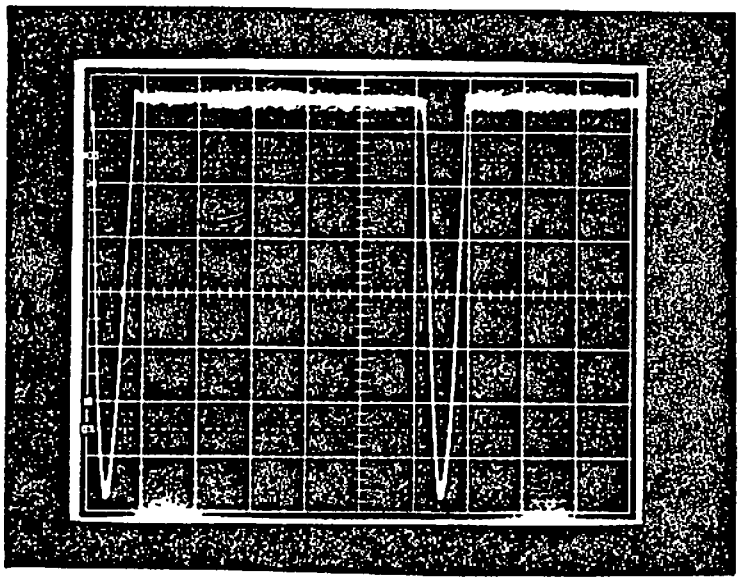


It can be seen that the deflecting coil current has a linear sawtooth or ramp waveform. The circuit action which gives rise to this current waveform has basically two components. On the one hand, there is an exchange of energy between capacitor C73 and the network of inductors in series with this capacitor, consisting of L4, L5, T7 and the deflection coil. The resonant frequency of this series circuit is a good deal lower than the switching frequency of the horizontal output transistor. Consequently, it is the current flowing in this circuit, having a relatively small and linear gradient, which constitutes the ramp part of the sawtooth.

On the other hand, there is an exchange of energy between capacitors C69 and C69A and the inductive network. These components effectively constitute a parallel circuit with a resonant frequency higher than the switching frequency. The current in this circuit has the steep gradient which is represented in the short return traces at the ends of the ramp.

Energy is supplied to these circuits from the core of flyback transformer FBT1. This transformer is connected to a 60V DC regulated supply through the emitter-collector path of the horizontal output transistor, Q23. The transformer core is charged (i. e., energy is stored in the form of magnetism) while Q23 is conducting. When Q23 is turned off, energy is released from the core (with the collapse of the magnetic field) and appears at the emitter of the transistor as a large voltage pulse. This flyback pulse is shown in the oscilloscope photograph reproduced below.

<u>Oscilloscope</u>
Sync - Int
Coupling - DC
Sweep - 10 usec/div
Vert - 100V/div



An operating cycle of the horizontal output stage begins when transistor Q23, an MJ12005, is turned on by a pulse from its driving stage. (This pulse has a duration of a little less than half the period of a full operating cycle). Q23's emitter is then raised to a potential about equal to the supply voltage (+60V). This voltage appears across the primary of the flyback transformer, FBT1, and current begins to flow in the primary winding. This current increases as energy is absorbed from the supply and stored in the transformer's core. At the same time, the voltage across the series LC circuit falls to near zero. Consequently, capacitor C73 begins to discharge through the inductive network which includes the deflection coil. (It is assumed that the capacitor was charged during the previous cycle of operation.) A current builds gradually in the coil as it absorbs energy from the capacitor.

When Q23 is turned off, the inductive circuit of L4, L5 and the horizontal deflection coil maintains current flow. This current decreases rapidly as it charges C69-C69A. The inductances and C69-C69A constitute a parallel resonant circuit of relatively high frequency. When Q23 is turned off, a damped oscillation at this relatively high frequency begins. As the current through the inductors continues in its original direction, C69-C69A charge to several hundred volts — the flyback pulse. The current through the inductors decreases to zero as C69-C69A reach peak charge. The CRT beams are swept back from right to screen center. As the oscillation contiunes, current through the inductors (including the deflection coil) reverses to continue the retrace toward the left side of the screen.

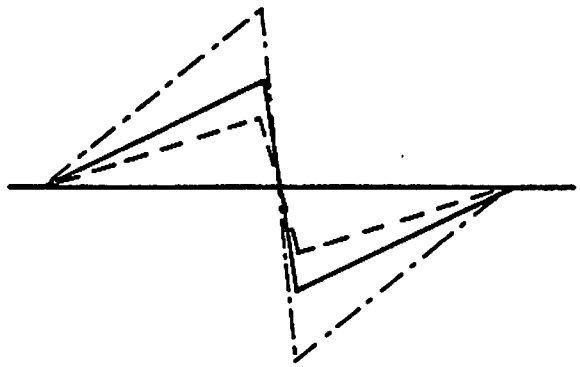
This current in the reverse direction discharges C69–C69A and would begin charging the capacitors in the opposite direction except for CR42. When the oscillation begins to enter the second half of its cycle, C42 becomes forward biased. As it conducts to kill the oscillation, the current flow through the inductors decreases toward zero, allowing the CRT beams to sweep in relative linear fashion from left toward screen center.

At this point another horizontal drive pulse turns on Q23 to begin another cycle of operation.

The shape and magnitude of the deflecting coil current are affected by the values of the components associated with the coil. The value of C73 is such that the ramp is not perfectly linear, but has a slight S curvature. This shaping of the current waveform is necessary to compensate for the distortion of the sweep by the curvature of the CRT screen.

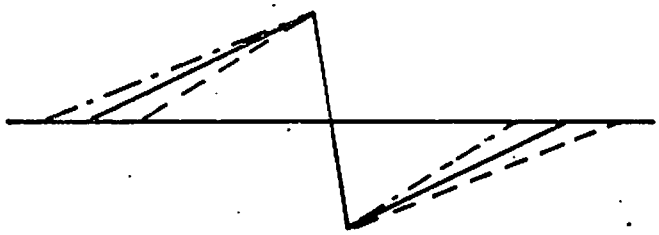
L5 is an adjustable inductor, connected in series with the deflection coil, which functions as a horizontal size or **width control.** As its inductance is varied the slope of the current ramp, hence the magnitude of the peaks, changes.

EFFECT OF WIDTH CONTROL (L5) ADJ. ON H-DEFL. COIL CURRENT



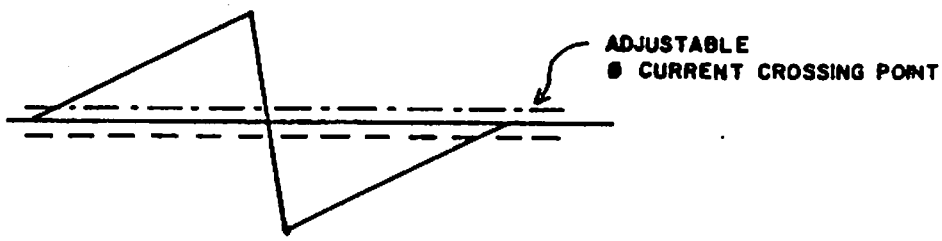
L4, another adjustable inductor in series with the deflection coil, functions as the horizontal **linearity control.** Adjustment of this coil does not affect its total inductance; it affects the coil's polarization. The permeable core is short relative to the length of the coil and can be offset from its center a little toward one end or the other. Accordingly, the gradient of the field strength in the coil can be changed. This gradient is adjusted to balance the current flow through the deflection coil. The quantity of energy transferred from the deflection coil as its current decreases (represented by the lower half of the ramp) should equal the quantity of energy transferred to the deflection coil as its current increases (represented by the upper half of the ramp). When this equality is established the ramp is straight; otherwise, it bends at the zero crossing point. The effect of a change in L4's polarization is represented graphically on the next page.

EFFECT OF LINEARITY CONTROL (L4) ADJ. ON H-DEFL. COIL CURRENT



T7, in parallel with the deflection coil, functions as an autotransformer in a dual half-wave rectifier circuit. This circuit is the source of an adjustable DC biasing voltage which is applied to the deflection coil for the purpose of centering the horizontal sweep. During the first and fourth parts of the cycle of the horizontal output stage's operation, induced voltages are present on the winding of T7 between pins 2 and 3 and between pins 3 and 4 which forward bias diodes CR43 and CR44. Capacitors C70 and C71 are then able to charge. C70 and C71 constitute two members of a bridge circuit, which is completed by a resistor chain made up of R106, R109 and R110. The DC voltage which appears across this bridge between the junction of the capacitors and the adjustable arm of R106 is applied to the deflection coil by way of T7 (that part of the winding between pins 3 and 6). The level and polarity of this voltage depend on the setting of R106. This control is adjusted to establish a direct current in the coil sufficient to compensate for differences between the center of the sweep and the center of the CRT screen.

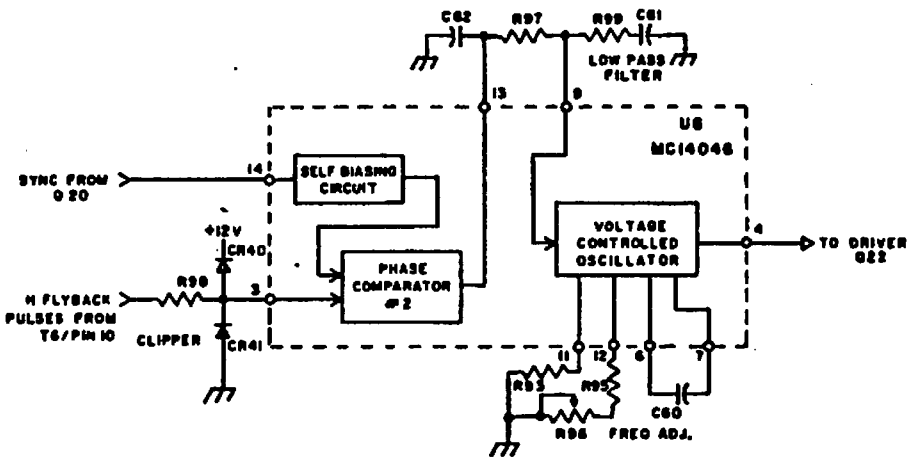
EFFECT OF H-CENTERING CONTROL (R106) ADJ.



The **horizontal driver**, consisting of an MC14046 integrated circuit, U6, a driver transistor, Q22, an NSD-U06, a driver transformer T5, and associated elements, furnishes the switching pulses for Q23 in the output stage. These pulses are frequency modulated, in order to synchronize the signal at the deflection coil with a signal supplied by the 5048 CRT controller in the display generator. Direct synchronization of the driving signal alone would not insure the proper timing of the horizontal sweep, because operating conditions in the horizontal output stage can vary considerably. Therefore, it is necessary that the output stage itself be under the control of the sync signal. In order to facilitate this control, the horizontal circuits have been organized into a phase locking loop. A sample of the deflection signal is returned to the driver and there compared with the sync signal. A phase difference between these signals results in a signal to the driver's oscillator which causes its frequency to increase or decrease and thereby compensate for the phase difference.

The driver's frequency modulator and oscillator are contained in U6, the MC14046 IC. A representation of the modulator and oscillator circuits is provided by the drawing below.

MC14046 AND ASSOCIATED CIRCUITRY



Square wave driving pulses are generated within U6 by a voltage controlled oscillator. The free running frequency of the oscillator is a function of the time constant of external capacitor C60 and external resistors R93, R95 and R96 in combination. The value of R96 is adjustable to give the proper operating frequency.

The voltage applied to the oscillator at pin 9 of U6 causes it to run at the frequency determined by the external RC elements or at some higher frequency. This voltage is supplied by a phase comparator within U6 through an external filter.

The phase comparator's output voltage is dependent on the phase relationship of the signals at its two inputs. The first of these signals is the synchronizing signal which originates in the 5048 on the logic board. The second is derived from the horizontal flyback pulses.

The 5048's signal consists of pulses which rise from ground level to about +5V for 3 to 4 microseconds at a frequency of near 16KHz. This signal, labeled HSYNCBL on the schematics, is routed to the deflection circuitry on the analog board by way of pin 2 in J5. The HSYNCBL signal is then applied to the emitter of Q20, a 2N4124. Q20 is employed as an amplifier (non-inverting) in a common base configuration, providing some voltage gain and a high output impedance to match the following circuitry.

Q20's output signal is applied (at pin 14) to a biasing circuit within U6. The sync signal is placed by this circuit at a level suitable to the phase comparator.

The second signal applied to the phase comparator is taken from pin 10 of the high voltage flyback transformer FBT1. The signal at this pin of the transformer consists of flyback pulses, smaller in amplitude than those at the deflection coil, but in phase with them. These voltage pulses are clipped by diodes CR40 and CR41 in route to the phase comparator.
CR41 conducts while the pulses are below ground level. The positive portions of the pulses above the level of +12V are clipped by CR40. The resulting signal is applied to the second comparator input at pin 3 of U6.

Proper operation of the phase comparator requires that the frequency difference between its two input signals be no greater than about 3.5 KHz. This is the range within which phase lock can be achieved. If, in a given cycle of operation, the rising edge of the HSYNCBL signal occurs before the rising edge of the clipped flyback pulse, the output of the phase comparator goes high during the interval between them. If the rising edge of the clipped horizontal flyback pulse occurs first, the comparator's output goes low. If the rising edges of the two signals occur simultaneously there is no output from the comparator.

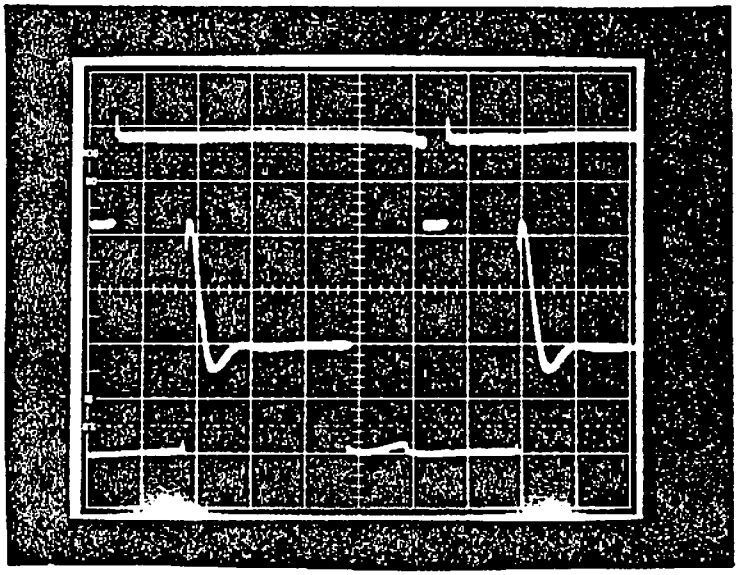
The comparator's output pulses are fed to an RC circuit consisting of C61, C62, R94, R97 and R99. This circuit is an integrator or low pass filter. It smoothes out the comparator's pulses, providing a continuously varying voltage to the oscillator in U6.

The oscillator's output signal is a 50% duty cycle square wave. This signal (at pin 4 of U6) is applied to the base of driver transistor Q22, an NSD-U06, through C64. Q22's output signal is in turn transformer coupled to the base of Q23, in the horizontal output stage. R105 and C66, tied to Q22's collector, help to shape the driving pulses. At the collector of Q22, the signal appears as a series of pulses with large spikes on their rising edges. The waveform is shown at the top of the next page.

The positive-going pulse seen at the collector of Q22 occurs when Q22 is not conducting. Transformer T5 is connected so that Q23 is driven into conduction during this time.

The driving signal at Q23's base remains low for a little over half the period of each operating cycle. It is during these times, when Q23 is not conducting, that C69 and C69A quickly charge and discharge and C73 charges. It is when the driving signal at Q23's base is high and the transistor conducting that C73 discharges.

Oscilloscope
Sync - Int
Coupling - DC
Sweep - 10 microsec/div
Vert - 2 V/div (upper)
10 V/div (lower)



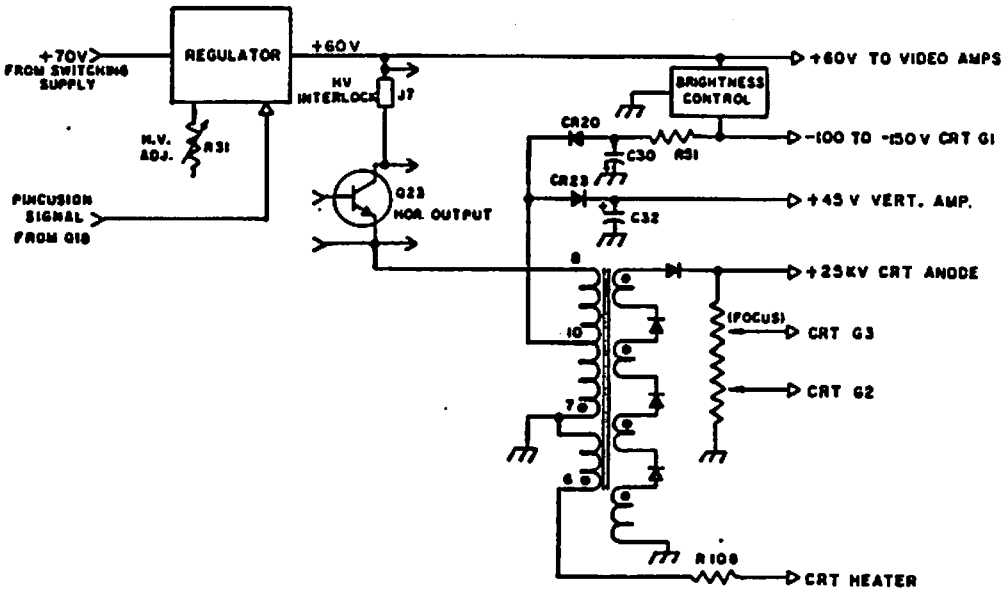
High Voltage Circuitry

The +70V output of the switching supply, described earlier, is fed to a conventional steady-state linear regulator which furnishes +60V to the video amplifiers and the horizontal output stage. The horizontal flyback pulses are, in turn, the basis both of the +45V used in the vertical amplifier and the high voltages and heater voltage for the cathode ray tube. The presence of the high voltages, CRT heater voltage and +45V is therefore dependent immediately on the proper operation of the horizontal output circuitry and beyond that on the the +60V output of the regulator. Provision is made in the regulator circuitry for the adjustment of the high voltages.

The regulator consists of transistors Q8, Q9 and Q10, differential amplifier U7, and their associated elements. The regulator's output voltage is monitored by U7, which makes the transistors more or less conductive in response to momentary drops or rises in this voltage due to load variations. U7 also responds to the pincushion signal from Q18 in the vertical deflection circuitry. Accordingly, it decreases slightly the conductivity of the transistors, and hence the output voltage, at times corresponding to the beginning and end of each vertical sweep.

A simplified diagram of the high voltage circuitry is shown at the top of the next page.

HIGH VOLTAGE CIRCUITRY



The non-inverting input (pin 3) of U7, a TL081, is tied to ground, which constitutes the reference point to which the signal at the inverting input is compared. A voltage divider, consisting of R30, R31 and R32, connected between the output of the regulator and the -12V line, provides one of two signals to U7's inverting input (pin 2). This signal is a voltage proportional to the regulator's output. The relation of this signal to ground can be adjusted by means of R31, which functions as an output voltage control. The pincushion signal is also applied to U7's inverting input. Thus U7's responses are the effect of the pincushion signal in combination with the signal derived from R31.

When the voltage at U7's inverting input goes negative in a negative direction, a positive-going signal results at its output (pin 6). Such a signal from U7, applied to the base of Q10, and MPS-A43, causes this transistor's conductivity to increase. An increase in Q7's collector current results, which causes an increase in the voltage across R28, making the base of Q9, an MJE350, more negative. Q9 is then more conductive, and the increase in its collector current results in an increased voltage across R29, which makes Q8's base more positive. Q8, a 2N3902 and the main regulating element, then becomes more conductive, and the output voltage rises.

When the voltage at U7's inverting input goes positive, a negative-going signal results at its output. In this case, Q8, Q9, and Q10 become less conductive, and the output voltage falls. CR14, connected between the base and the emitter of Q10, prevents U7 from turning the transistor completely off and thereby interrupting the current supplied by the regulator. When U7's output goes so low that its value approaches that of Q10's emitter voltage, CR14 conducts, preventing Q10's base from being driven more negative.

The +60V from the regulator is routed to the video amplifier circuits by way of pin 6, J8 on the analog board. This +60V is also used in the horizontal output stage. It is applied to the primary of the horizontal flyback transformer FBT1 through Q23's emitter-collector path.

When Q23 conducts, a portion of the applied +60V appears at pin 10 of FBT1. This causes CR23 to conduct and charge C32 to approximately +45V for use in the vertical deflection amplifier. The negative-going flyback pulse that occurs when Q23 is turned off is fairly large. So CR32 must have a high inverse voltage rating.

During the time Q23 conducts, current builds up in the primary of FBT1, storing energy in the form of a magnetic field. When Q23 is turned off, the stored energy causes a negative-going flyback pulse to be developed across the primary of FBT1. A portion of this at pin 10 causes CR20 to conduct to charge C30 to approximately -500V.

C30 supplies current through R51 to a 100V Zener diode, CR22, which is associated with the brightness control.

The **brightness control**, R115, mounted on the 2400's rear panel, is part of a network of resistors, including R54 and R55, which provide a variable bias to the cathode of CR22. The biasing voltage is derived from the +60V line and is adjustable between 0V and about +50V. Accordingly, the voltage at the anode of CR22 is adjustable between about -50V and -100V. This voltage is applied to the **control grid (G1) of the CRT.**

The **CRT heater voltage** is taken from a secondary winding of FBT1 at pin 6 of the transformer. Pin 6 furnishes about 20V peak-to-peak with respect to ground. The duty cycle is such as to result in approximately 6.3 volts RMS.

The main secondaries of FBT1 are connected in series with diodes that are included within the transformer package. The output of this secondary circuit is about +25KV, depending on the setting of R31 in the +60V regulator. This voltage is applied to the **CRT anode.**

A heavily insulated voltage divider, which provides two adjustable outputs, is connected across the +25KV line. Adjustment of the upper (more positive) tap controls the **focus** of the CRT beams, since this tap supplies the voltage for the **CRT's third grid** (G3). This voltage is variable between about +6.5KV and +7.5KV.

Adjustment of the lower (less positive) tap controls the **CRT's second grid** (G2). This control is set to obtain a CRT beam current of 500 microamps with a white raster at full brightness. The voltage at the CRT's second grid under these conditions is typically about +230V.

Overcurrent / Undervoltage Circuit Modifications

The latching action of Q1, outlined in the undervoltage/overcurrent circuit description, existed in early 2405 terminals. It probably does not exist in any 3600 Series units. Because of the inconvenience of physically operating the unit power switch off and then back on following any momentary power interruption, the circuit was modified by removal of Q1 and R3. R2 then was tied to the collector of Q2 as shown on schematic drawing 102350. This change probably was introduced prior to the use of this analog board in 3600 Series units.

However, without the latching feature, momentary power interruptions sometimes resulted in other problems, including circuit failures -- in 2400 Series or 3600 Series units. A second modification, involving a small printed circuit board, was made available in the last quarter of 1984.

The "Auto Restart" modification provides a delay in restart after a momentary power interruption and beefed-up overcurrent circuitry. The circuits on the added PCB are shown on schematic drawing 103387. The associated installation drawing shows how the board is placed and connected.

In the modification, Q3, R23, R41 and CR10 are removed. This effectively eliminates U3, Q2, Q3 and associated components from the circuit. Leads from the added PCB connect the added PCB's R19 in the place formerly occupied by R23. Current drawn by main switching transistor Q7 passes through the small PCB's R19. A portion of this current also passes through the parallel path of the added PCB's R18, R17 and LED part of U2.

The collector of Q2 on the added PCB is connected to the point formerly occupied by the collector of Q3 on the main board -- to terminal 10 of U4. If excessive current is drawn by the switcher, the transistor part of U2 on the added PCB conducts enough to turn on the added board's Q1, which turns off the added board's Q2. The resulting high at the collector of Q2 shuts down U4, the pulse generator for the main switcher.

This portion of the added board differs from the earlier version on the main board principally in having greater adjustment range and in limiting current to a lower value in case of Q7 short. The first point results in adequate adjustment range, the second in prevention of extensive damage to components in the overcurrent circuit.

The added PCB's U1 and associated components provide a delay in switcher start-up after a power interruption. U1 is configured as a monostable multivibrator. The timing elements R31 and C1 provide an output pulse of approximately 3.6 seconds duration. This positive pulse turns on the added board's Q3 to bring its collector near ground. Q3's collector is connected through CR1 to terminal 9 of U4 on the main board -- at the point formerly occupied by the anode of the main board's CR10. The resulting low at U4 pin 9 effectively shuts down the pulse generator.

The added PCB has connections to the main board's +5V, +12V and ground via a cable to the main board's J11.

At unit power-up, on the added board the initial rise of the +12V supply is coupled through C4 to the base of Q4. Q4 turns on briefly to result in a negative-going pulse, coupled through C6 to pin 2 of U1. This triggers U1 and the output pulse of U1 holds off operation of the analog's main switcher for a few seconds. Then normal operation begins.

During normal operation, the added board's CR3 provides limitation of the switcher's pulse width in the same way that the main analog board's CR19 accomplished this limitation formerly.

If the +5V supply should drop below +3.3V, Q6 on the added board turns off. The resulting positive-going signal at the collector of Q6 is coupled through C5 to turn on Q5 briefly. The negative-going pulse at the collector of Q5 triggers U1 to shut down the main switcher for several seconds.

Normal operation, with the +5V supply up, causes the LED on the added board to light. When +5V is lost, the LED is extinguished.

VIDEO AMPLIFIERS AND CRT — In-line Version

The video amplifiers are situated on a small printed circuit board mounted vertically at the base of the CRT. In the circuit descriptions which follow, reference is made to components in accordance with the nomenclature of schematic drawing 102700 (Revision 2 board.) The 3600 Series units use the "one bit" version of the board. Jumper W1 is installed. The gain controls are 50-ohm potentiometers. (See table at right side of schematic drawing.)

Connections to the CRT socket, mounted on the Video Driver PCB, include those for the CRT heater, focus, G2 bias and G1 bias. All of these voltages are developed in the Analog Module. The video signals are applied to the three CRT cathodes.

Red, green and blue video signals at TTL level, active low, are brought in from the Logic Module at J2. The video driver assembly contains three amplifiers, one for each of the CRT's three electron guns. Each amplifier accepts one TTL input from the display generator in the Logic Module and provides a two-state output to turn its gun on or off ("one-bit" video). When no video pulses are present at the amplifier inputs, the outputs drive the CRT gun cathodes sufficiently positive to the to keep the guns turned off. When video pulses appear, the amplifier outputs drive the gun cathodes mtoward ground level, allowing the guns to emit electrons.

Each amplifier is equipped with a gain control to permit independent adjustment of this voltage swing at each cathode, which is necessary for color balance. The controls are labeled R17, R6 and R3, for red, green and blue respectively, and are easily accessible upon removal of the terminal's cabinet cover.

The three amplifiers are essentially the same, and the description of the red gun amplifier which follows is applicable to the others with appropriate changes in componeent nomenclature.

The red gun amplifier consists of a driver and a class B power amplifier. The driver is U1, a 75451B dual AND gate with high current capacity open-collector outputs. Power amplification is handled by Q1, an NSD-U06 transistor, operating in the common base mode. The base voltage is set at +5V (+/- 5%) by voltage regulator VR1.

Red video signals are supplied to the input terminals of the driver by the display generator on the 3600 logic board. These signals are negative-going pulses. The red driver's input terminals are high (about +5V) when there is no video and the red gun is to be turned off; they are low (about ground level) when video is present and the gun is to be turned on. A high at the driver's inputs allows the transistor at the driver's output stage to conduct relatively little collector current. A low allows the transistor to conduct a relatively large collector current.

The collector of the driver's output transistor is connected (by way of pin 3 of U1) to Q1's emitter through R16 and R17. A fixed bias of +5V is applied to Q1's base. When the signal at the driver input is high, a high impedance appears in Q1's emitter circuit, its base-to-emitter voltage is close to zero, and it is cut off. Consequently, the voltage drop across its collector load resistor R8 is quite small, and a potential very nearly as large as Q1's collector supply voltage (+60V) is present at the red gun cathode. This potential is sufficiently positive to keep the gun off.

When the signal at the driver inputs goes low, Q1's emitter voltage is pulled down by the conduction of the driver's output transistor. Q1 is then turned on and can then conduct a large collector current. This current flow is accompanied by a large voltage drop across R8, and the red gun cathode is pulled toward ground. Consequently, the red gun is turned on. The conduction of Q1 is controlled by the setting of gain control R17, the individual color brightness control.

Inductor L1 in series with the collector load resistor extends the amplifier frequency response to provide good response to the video "dot" signals. The fundamental frequency of the video is near 9 MHz and the signals have fairly fast rise and fall times.

Note that one-bit operation is established by installing jumper W1, and installing 50 ohm gain controls (R3, R6 and R17). Resistors R18, R21 and R22, and bias controls R1, R4 and R15 are not installed.

The CRT now used in the 3600 Series terminals has in-line guns and medium-short persistance phosphors. The characteristics of this tube permit the realization of the best possible raster resolution consistent with the use of 60Hz non-interlaced vertical scanning and economical display generator logic. Non-interlaced scanning is highly desirable because it provides superior picture brightness and color definition with a minimum of flicker.

In an in-line tube such as this, the convergence of the beams at a given "dot" can be maintained throughout the sweep with a minimum of focusing equipment. Permanent magnets positioned on the neck of the tube are sufficient. The constant orientation of each beam toward a particular type of phosphor (purity) is also maintained with permanent magnets, as is the case with most CRTs.

The horizontal drive signal, supplied by the Analog Module, has been modified to maintain straight columns. The CRT itself maintains straight rows — vertical pincushion adjustment is not required.

The tube's convergence and purity magnets, along with its deflection yoke, are installed and aligned by the tube manufacturer. These components are permanently bonded to the tube neck in the proper positions. Field adjustments are not required, and attempts to remove or reposition these components can be hazardous.

COMPUCOLOR II CIRCUIT DESCRIPTION

The Compucolor II circuit components are contained in a TV-type cabinet and a separate keyboard. The major subassemblies are:

CRT & Cabinet	8-color visual display and unit housing.
Power Assembly	Conversion of 115VAC to unregulated DC, low voltage AC and line frequency sync.
Analog Assembly	Regulated voltages for system; CRT sweep and convergence currents; bias, focus and anode voltages.
Logic Assembly	Data programs and processing for control of video display; sync signals to Analog.
Video Assembly	Amplification of video signals from Logic; CRT connections and bias adjustment.
Disk Drive	Data storage and retrieval.
Keyboard	Manual data input and control.

The keyboard essentially is the same as that described for the 3600 Series on page 5.43. The keyboard cable terminates in an edge connector.

The micro-disk drive is the same as that used in the 3621. Its circuit description begins on page 5.40.

The logic board also is the same as that used in the 3621. Its circuit description begins on page 5.29.

The CRT was made to Compucolor specifications, 13" diagonal in-line (but not pre-converged). Consult Intecolor applications engineers if replacement is required.

The circuit descriptions for the power board, the analog board and the video board are given on the following pages taken from the original Compucolor II Maintenance Manual. Notes regarding analog board modifications are included at the end of the section.

V. SUBASSEMBLY DESCRIPTIONS

A. CRT, YOKE and CABINET

The Compucolor II 8-color display unit is a 13 inch cathode ray tube 13VAXP22. It is secured in the cabinet by a spring harness and has a yoke assembly containing the deflection and convergence coils. The CRT and yoke are similar to standard TV components.

Connections to the CRT are through a socket on the Video Board and two HV leads. Connections to the yoke assembly are through connectorized cables from the Analog Board.

The required voltages and signals for the CRT have sources as follows:

Filament voltage -	6.3 VAC from the Power Board via the Video Board.
Screen control -	200 VAC from the Analog Board and adjusted by three potentiometers on the Video Board.
Cathode return -	Through a common resistor on the Video Board to ground.
Video input -	Signals from the Logic Board through driver amplifiers on the Video Board to CRT control grids.
Focus voltage -	Approximately 4KV by separate lead between CRT socket on Video Board to HV Supply attached to Analog Board. Fine adjustment potentiometer mounted on Analog Board frame.
Anode -	20KV by separate lead from HV Supply on Analog Board to CRT HV connector.

Deflection and convergence currents for the yoke assembly are developed in the Analog Board from timing pulses supplied by the Logic Board.

B. POWER BOARD

The Power Board is mounted in the rear cover of the cabinet. Its circuit is shown in the upper right portion of Analog Schematic Drawing 100902 (or 100903). It supplies unregulated 150 VDC and 15 VDC, 6.3 VAC and Vertical Sync. The 3 - wire power cord for 115 VAC input connects to this unit. Line fuse F1 (2.5 A.,slow blow) is located on the Power Unit. The ON-OFF switch SW 1 is mounted on the Power Board and is operated from outside the back of the cabinet. There is a line filter. Varistors protect against voltage spikes.

+150 VDC is supplied by bridge rectifier BR2, with filtering by capacitor C2. The +150 VDC source has additional fusing in F2 (1.5 A., fast acting) located in the Power Unit.

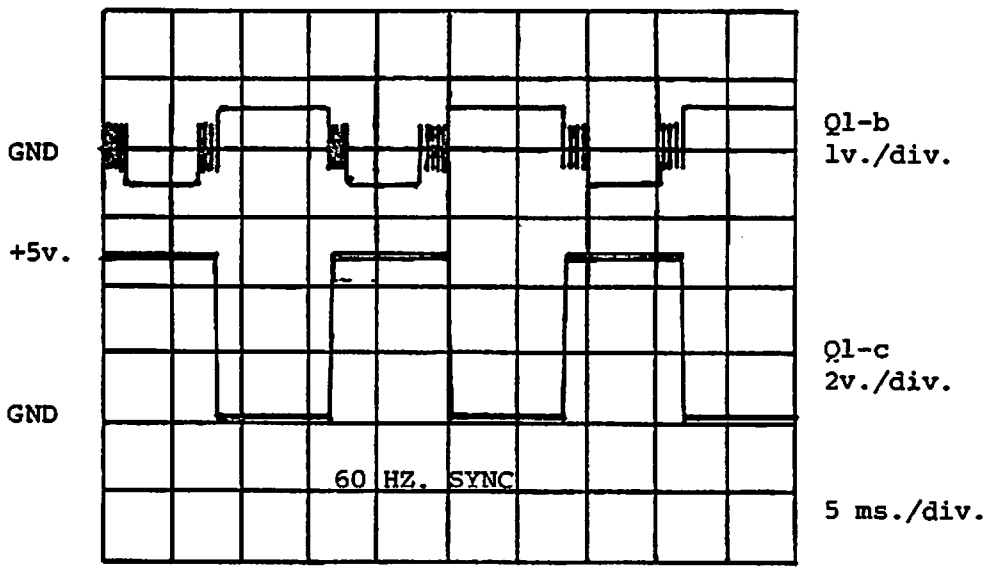
CAUTION: Note that the +150-volt supply is not referenced to frame ground. It has a "hot" common. Special precautions are required for measurements.

The +150 VDC is used directly in the horizontal sweep circuit and the switched regulator on the Analog Board and indirectly, via the switched regulator, in almost all other parts of the system.

+15 VDC is supplied by bridge rectifier BR3, with filtering by capacitor C7. AC input to the rectifier is from the full secondary of stepdown transformer T1. The +15 VDC supply is referenced to frame ground. +15 VDC is used directly in the horizontal sweep circuit and the switched regulator on the Analog Board. Failure of the +15 VDC supply will result in loss of the regulated voltages required by most parts of the system.

6.3 VAC for the CRT filament is supplied by one-half the secondary winding of stepdown transformer T1. It is connected to the CRT through the Video Board.

Vertical Sync Generator Q1 is located on the Power Board. Low voltage 60 Hz. from transformer T1 is applied to the base of Q1 through current limiting resistor R2. The negative-going portion of the waveform is clipped by diode CR1 and the positive-going portion by the transistor base-emitter junction. The collector load resistor and supply voltage are located in the Analog Board. The collector output rectangular waveform goes to the Logic Board by way of the Analog Board.



Waveforms at F2 and C7+, though not shown, are essentially DC with noise and ripple normally 6.0 and 1.0 volts peak-to-peak respectively.

C. ANALOG BOARD

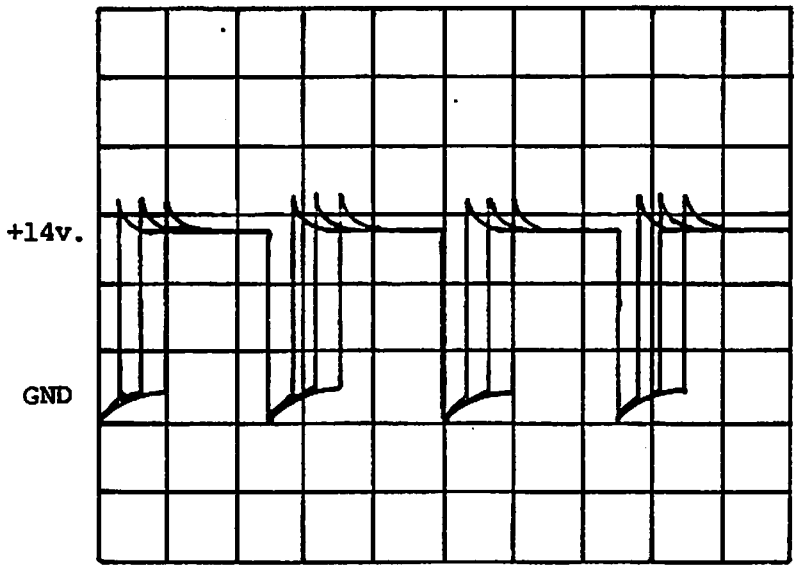
The Analog Board is mounted in the side portion of the Compucolor II cabinet, beside the CRT. It provides regulated low voltages used throughout the system, horizontal and vertical sweep currents and convergence signals for the CRT yoke assembly, and 200 VDC for the CRT screen controls. A high voltage unit attached to the Analog Board supplies the CRT focus and anode potentials. The Focus potentiometer is mounted in the frame of the Analog Board. Schematic Drawing 100902 shows the circuits involved.

Regulated low voltages are developed by a switching regulator from unregulated 150 VDC and 15 VDC furnished by the Power Board. The right hand side of the Analog Schematic shows the circuit.

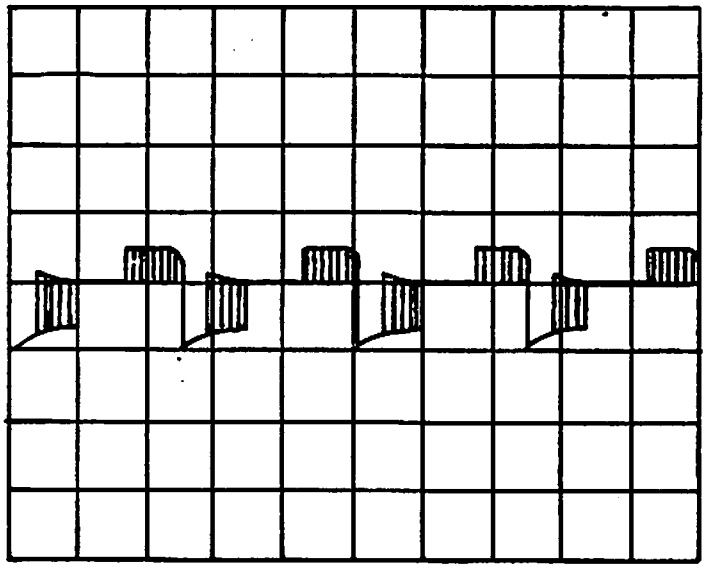
U3 and associated components generate a square wave at approximately 20 KHz. to drive power amplifier transistors Q6 and Q7. These transistors provide the input to transformer T4. The T4 secondary delivers the 20 KHz. square wave at several voltage levels to bridge rectifiers BR1 and BR2 and to full-wave rectifier CR3 and CR4. Regulation is achieved by control of the supply voltage to Q6 and Q7. U2, Q5 and associated components perform this function.

U2 generates a variable-width pulsed waveform (approximately 20KHz.) to control the duty cycle of Q5. The pulsed waveform applied to the Q5 base-emitter junction causes Q5 to conduct for the positive-going pulse duration. Since Q5 is in series with the voltage supply to Q6 and Q7, widening of the positive-going pulse causes Q5 to conduct a greater portion of the time and increase the nominally 100VDC supply to Q6 and Q7. When the positive-going pulse is made more narrow, the supply to Q6 and Q7 is decreased. Feedback from the +5V Regulated output at BR1 causes U2 and Q5 to adjust the supply to Q6 and Q7 as required to keep the +5V Regulated level constant.

U2 and U3 are SG3524 integrated circuits requiring input DC in the range of 8 to 40 volts across pins 15 (+) and 8 (-). In this instance both U2 and U3 have pin 8 at frame ground and pin 15 to +15VDC from the Power Board. One output, at pin 16, is a well regulated nominally +5VDC; it is used as a reference in control of the switched regulator but also is available for other usage in currents up to 50 mA. The frequency of the U2 pulsed output is controlled by R24 and C4. The positive-going pulse time is determined internally by comparison of a portion of the feedback voltage (at pin 1) to a portion of the reference voltage (pin 2). R22 provides feedback adjustment and is used to set the +5V Regulated output at the correct level. The output variable-pulse-width waveform is available across collector-emitter combinations CA-EA (pins 12 & 11) and CB-EB (pins 13 & 14). In the case of U2, the connection to the primary of transformer T2 is from only the CA-EA combination.



The U2 - generated pulses applied to Q5 through T2 results in Q5 being turned on for varying portions of the waveform period. The Q5 output is a chopped DC waveform, which is filtered by L1 - C34.



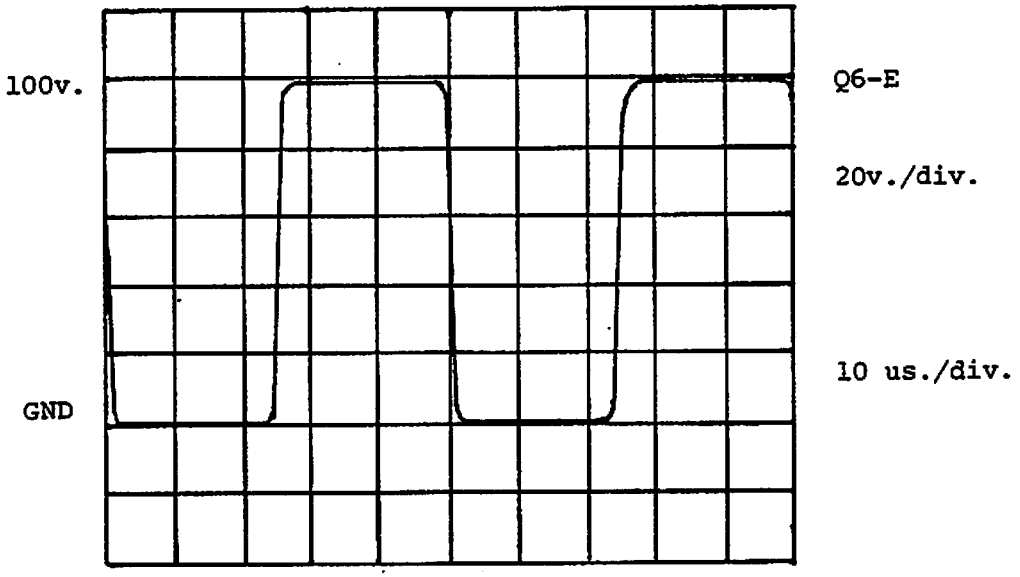
U3 also generates a rectangular waveform, with output connections at terminals 11 through 14, but its circuit differs from that of U2 in two respects:

1) Both output combinations CA-EA and CB-EB are used to drive transformer T3.

2) The feedback is fixed to yield a symmetrical square wave at the output.

R44, R45 and R43 provide the references to obtain the square wave. R47-C28 set the frequency to approximately 20 KHz.

The 20 KHz. square wave is applied to the primary of T3 to drive push-pull amplifier transistors Q6 - Q7. The amplitude that these transistors deliver to the primary of transformer T4 is dependent upon the momentary level of the supply voltage at Q6-C. This voltage, as described earlier, is regulated by U2-Q5 to be the level required to keep the +5V Regulated output constant.



The regulated low-voltage DC outputs are obtained from rectifiers BR1, BR2 and CR3-CR4, each with output filtering. Although feedback from only the +5V Regulated is used for voltage control, the loads on the other outputs are sufficiently stable to consider these other voltages also regulated. All of these voltages are referenced to frame ground. They supply circuits as follows:

-48 V. Video Board driver amplifiers.
Analog Board horizontal and vertical ramp reset circuits.

±12V. Logic Board circuits
Analog Board horizontal and vertical ramp, parabola and pincushion circuits.

±11-volt outputs through resistors R50 and R51, with additional filtering for the convergence and vertical sweep amplifiers.

-8-volt reference through VR1 for ramp generators.
+8-volt level through voltage divider R91-R98 for the convergence signal switches in U5.

±5V. Logic Board circuits.
CRT cathode bias

In addition to the voltages listed above, there are two other reference voltages, with lower current capabilities, used in the Analog Board:

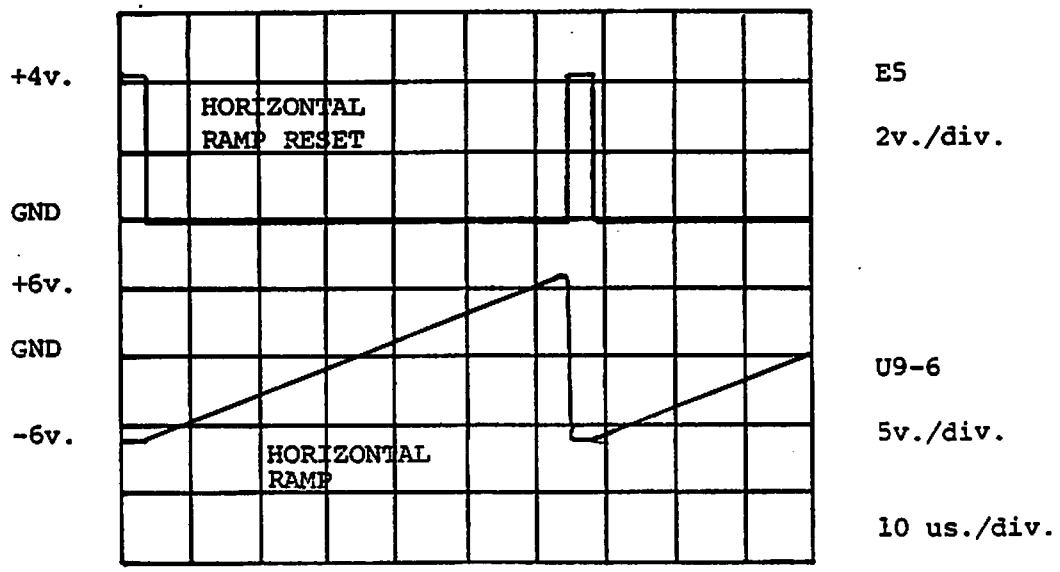
+5V. REF1 From U2-pin16. Referenced to frame ground. Used in the horizontal sweep generator, the vertical sync generator (collector supply for Q1 on Power Board) and the horizontal pincushion optical coupler.

+3.9V.REF2 From CR3. Referenced to 150V "hot" common. Used in horizontal sweep generator circuits.

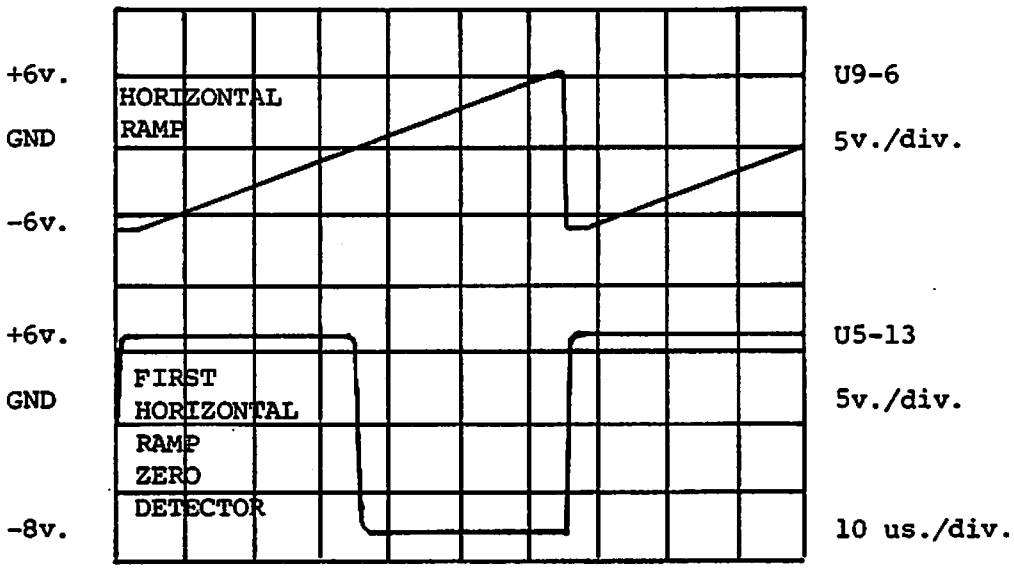
None of the regulated low voltages and reference voltages should have noise or ripple exceeding 3 % other than the ±11V. supply for the vertical sweep amplifier.

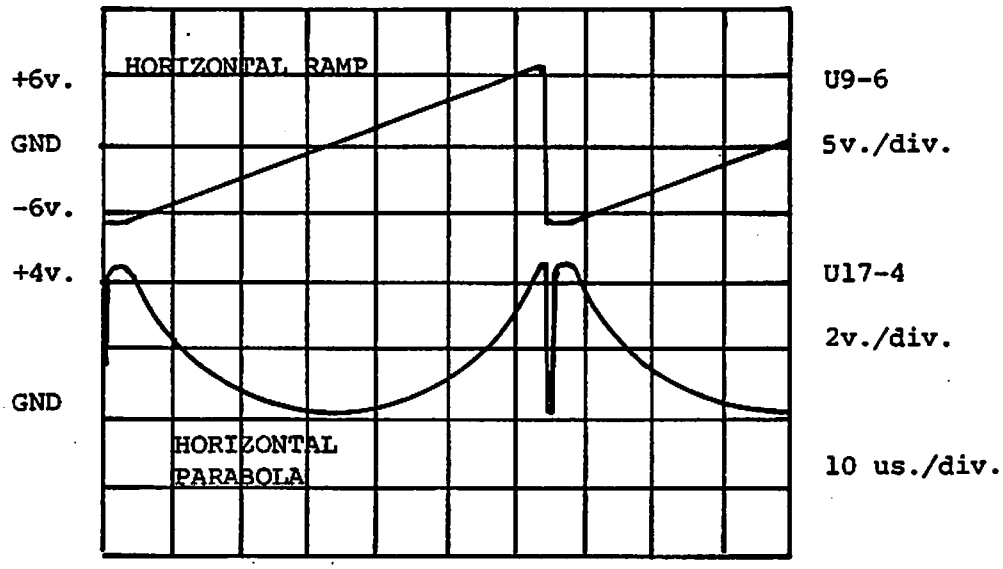
Convergence Circuits are shown in the upper left portion of Analog Schematic 100902. These include horizontal ramp and parabola, vertical ramp and parabola, pincushion, switches to develop signals for each of four quadrants, and a convergence amplifier.

The horizontal ramp sawtooth is generated across capacitor C48 by operational amplifier U9. The rate of voltage rise across C48 is adjusted by R102 to equalize the ramp positive and negative points at U9-6. The steep discharge portion of the sawtooth occurs when FET Q13 conducts. Normally the E111 is biased off by the -48V. through R59 and CR17. However, when the Horizontal Ramp Reset pulse from the Logic Board causes Q12 to conduct, the resulting positive-going pulse at the Q12 collector is coupled by capacitor C47 to the gate of Q13 to turn on the FET for discharge of C48. As soon as the reset pulse has passed, the -48V. again biases Q13 off and the linear charge of C48 begins anew. The waveform at U9-pin6 is a linear sawtooth with a period of approximately 65 us.

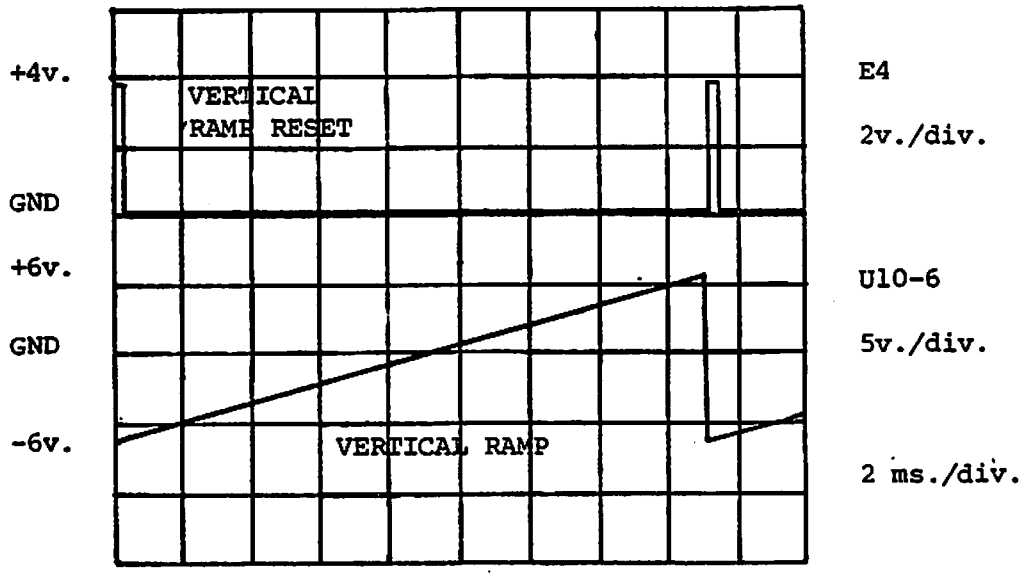


This horizontal ramp is passed through comparators in U8 to apply square waves to pins 5 and 13 of the bilateral switches in U5. Pin 13 is positive during the first half of the ramp, pin 5 during the second half. The horizontal ramp also is connected to the input of analog multiplier U17 to develop the horizontal parabola applied to other inputs of U5 at pins 2 and 3. (The output at pin 4 of U17 is one-tenth of the product of the two inputs at pins 1 and 6. Since the horizontal ramp - call it "X" - is applied to both inputs, the output - call it "Y" - then is $Y=X^2/10$, the formula of a parabola.) R102 is adjusted to equalize the amplitude of the right and left parabola end points. R101 is used to adjust the DC offset of the parabola to bring the parabola center to ground.



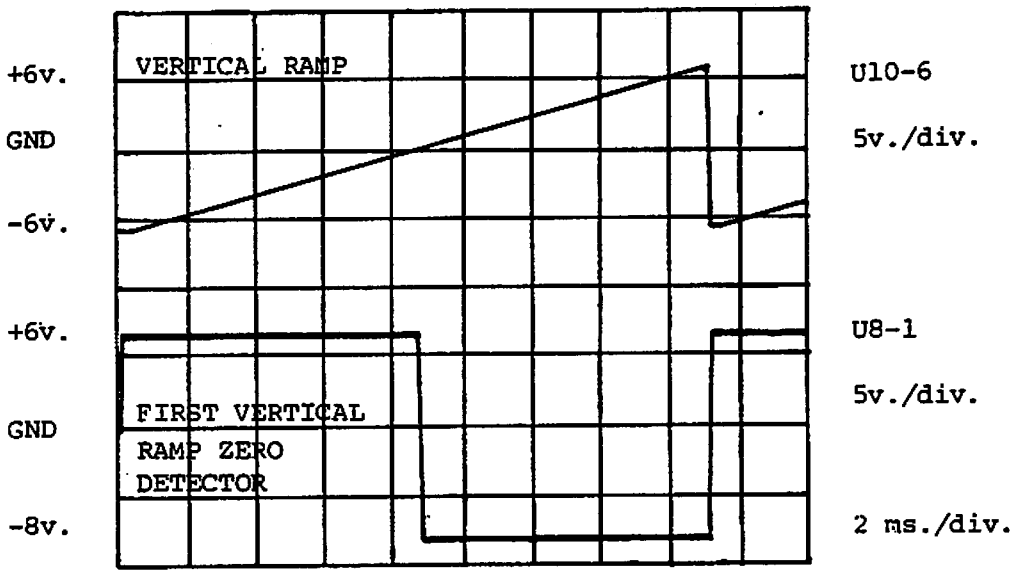


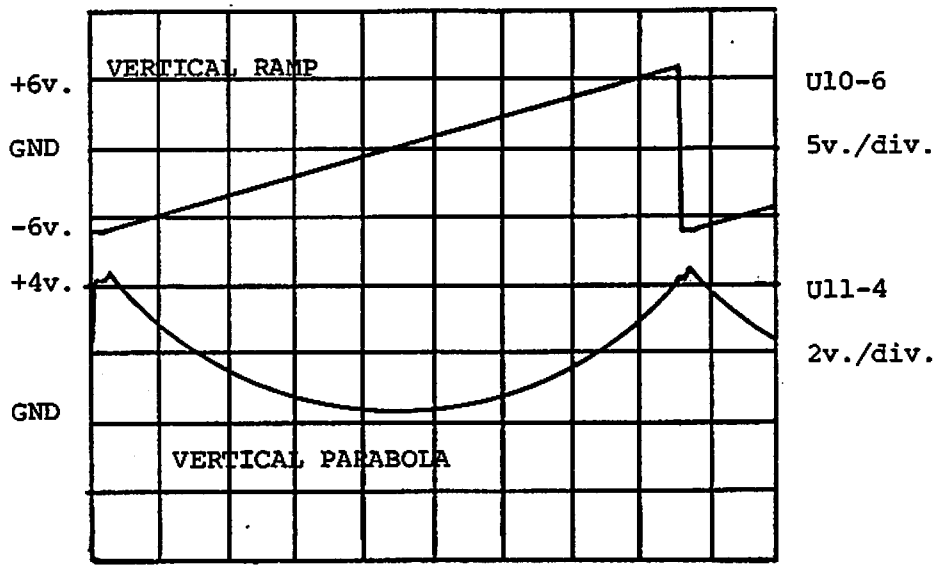
The vertical ramp and parabola are generated in similar fashion. Operational amplifier U10 requires more time to charge the larger sweep capacitor C50. The charging rate is adjusted by R103. The wider Vertical Ramp Reset pulse through Q14 to FET Q15 results in longer turn-on of Q15 and a slight dead time between C50 discharge and initiation of the next ramp. However, this dead time is a very small percentage of the total ramp time and is less noticable in the vertical than in the horizontal ramp.



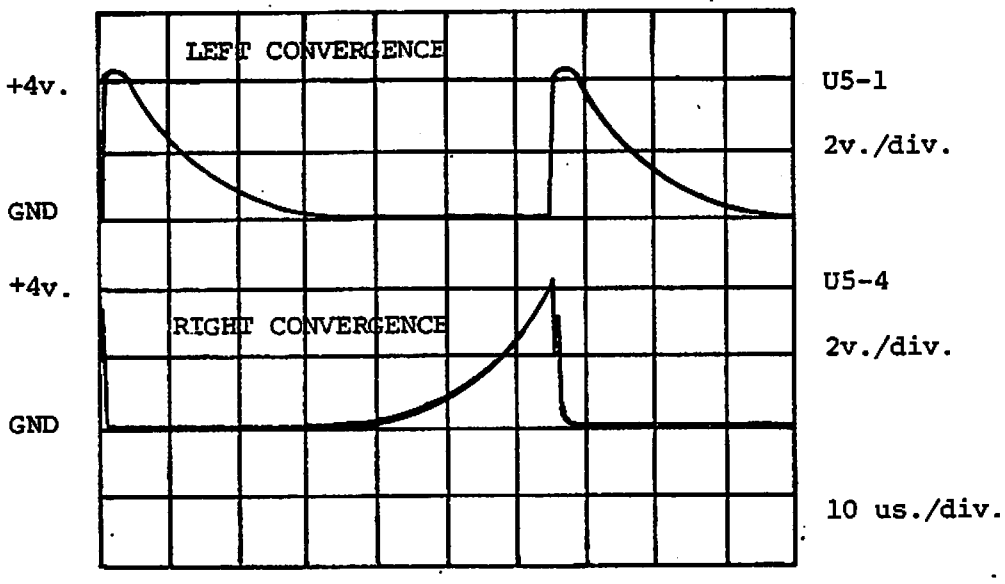
The vertical ramp is also passed through comparators in U8 to switches in U5, with pin 6 of U5 receiving a positive signal during the first half of the ramp and pin 12 a positive signal during the second half. The vertical parabola is applied to other inputs at pins 9 and 10.

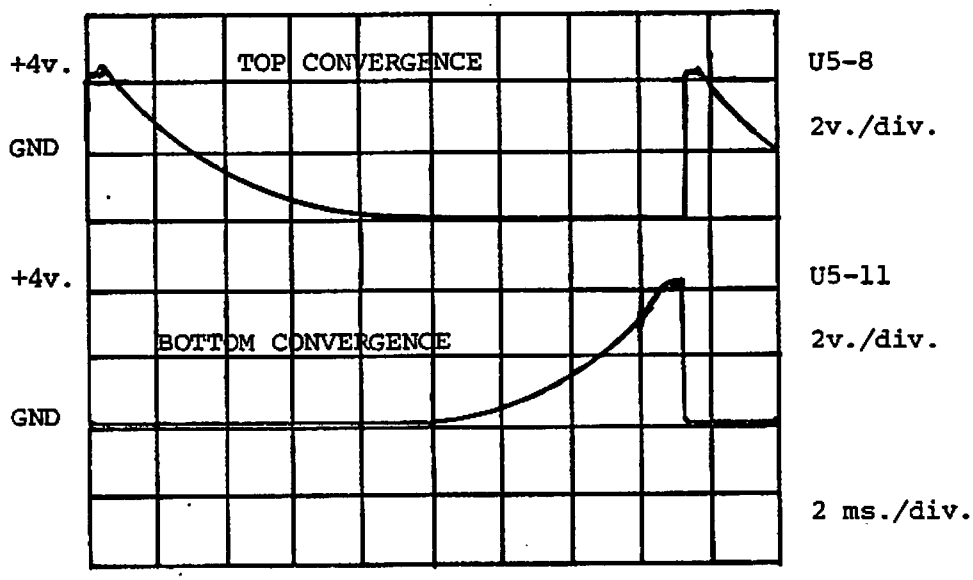
The vertical parabola is developed in U11. Adjustment of R103 equalizes the heights of the parabola end points. Adjustment of R104 brings the parabola center to ground level.


+6v.
GND
-6v.
+6v.
GND
-8v.
VERTICAL RAMP
FIRST VERTICAL
RAMP ZERO
DETECTOR
U10-6
5v./div.
U8-1
5v./div.
2 ms./div.


+6v.
GND
-6v.
+4v.
GND
VERTICAL RAMP
VERTICAL PARABOLA
U10-6
5v./div.
U11-4
2v./div.

Power supply for all four U5 switches is +8V. from R98-R91 to U5 pin 14, and -8V. from VR1 to U5 pin 7. The combination of square wave and parabola waveforms at the switches result in the convergence waveforms.

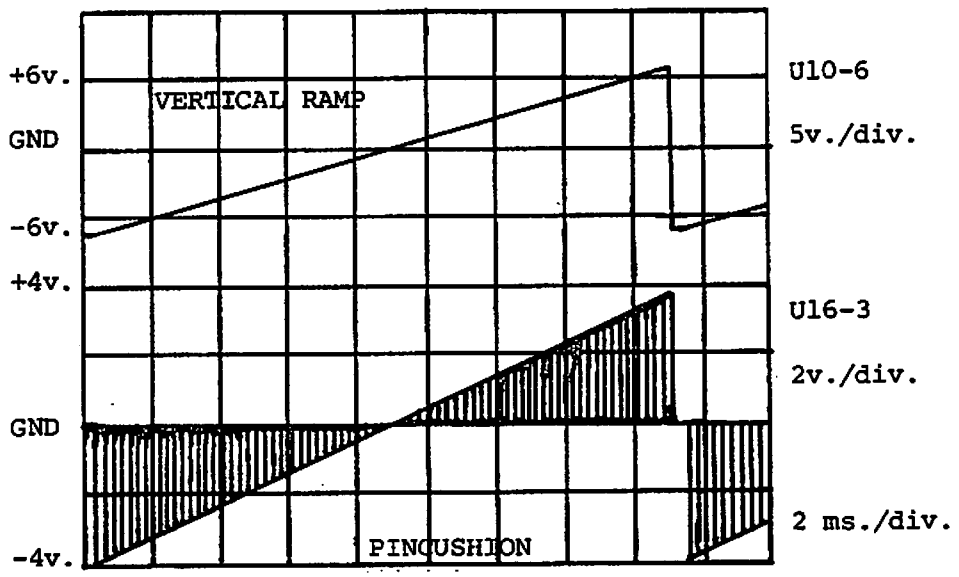




These waveforms from U5 are summed in proportions determined by the adjustments of convergence RIGHT, LEFT, TOP and BOTTOM control potentiometers R95, R94, R96 and R97 and applied to the input of power driver U13.

U13 provides amplification to drive the power amplifier transistor Q17, which has the convergence coil in the CRT yoke assembly as a load. Power supply for both U13 and Q17 is 11 volts. Feedback is provided by R75-C66 and by R76.

The vertical ramp and the horizontal parabola are combined in analog multiplier U16 to produce the pincushion waveform used in the vertical sweep generator.



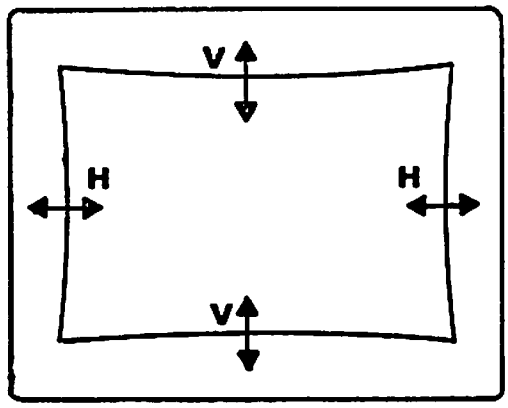
(Horizontal Parabola multiplied by Vertical Ramp)

Vertical Sweep is developed in the circuit shown in the center left portion of Analog Schematic 100902. Power driver U12 receives two signal inputs. The vertical ramp sawtooth input amplitude is adjusted by VERT HEIGHT potentiometer R106 and the pincushion input by VERT PINCUSHION potentiometer R107. The vertical ramp is the basis for vertical sweep. However, it is modified by the pincushion signal to yield equal deflection across the top and bottom of the CRT display.

In the CRT the electron beam travels farther to reach the top corners of the display than it travels to reach the top center. Therefore, for a given amount of angular deflection vertically, the beam strikes the CRT face higher at the top corners than at the top center.

V = Vertical
Pincushion

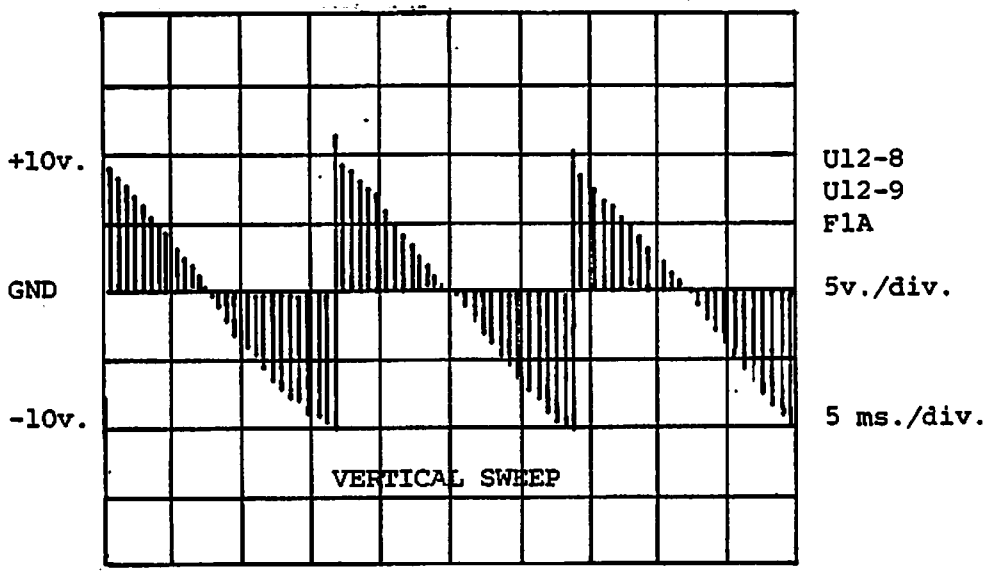
H = Horizontal
Pincushion



Vertical pincushion compensates by slightly reducing vertical angular deflection progressively as the position of the beam horizontally departs from center. The CRT display then has uniform vertical deflection across the top and bottom.

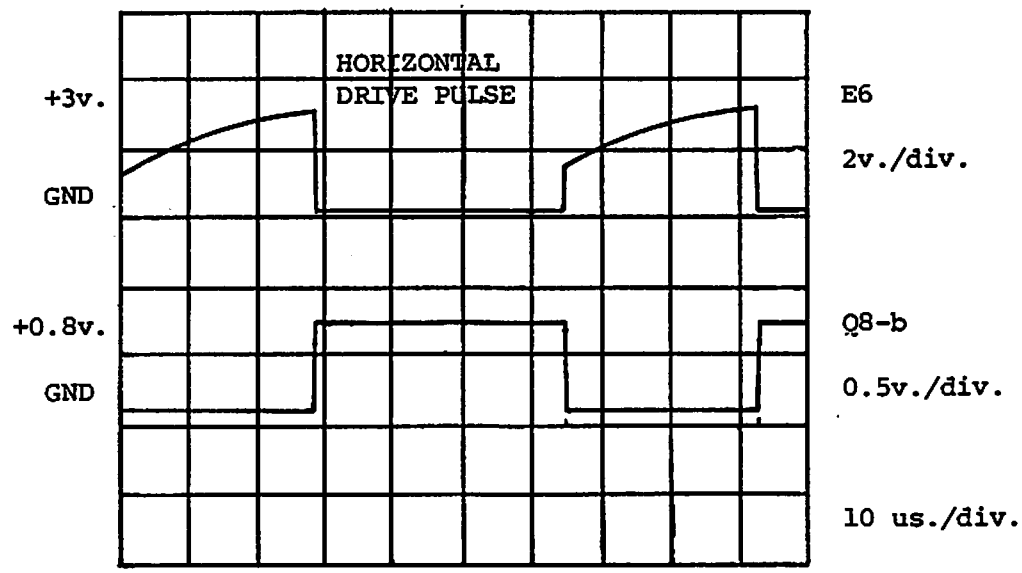
The U12 combines the two inputs and produces two composite outputs to drive power amplifier transistors Q18 and Q19.

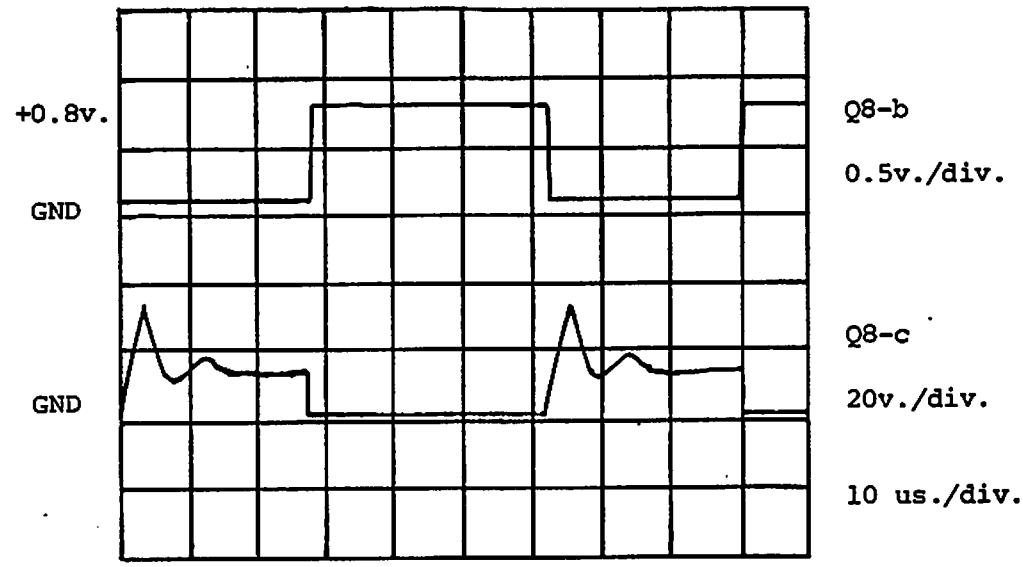
Vertical centering of the sweep waveform is accomplished by adjustment of VERT CENTERING potentiometer R105. Frequency compensated negative feedback to insure linear amplification is applied to pin 4 of U12 from both the power amplifier (network R73-C62-C67-R72) and the vertical deflection coil (via R71). The power amplifier transistors Q18-Q19 have the vertical deflection coil as load. Series protection against shorts is provided by fuse F1A (1.5 A.).



Horizontal Sweep circuits are shown in lower left portion of Analog Schematic 100902.

Sweep timing is furnished by the Horizontal Drive Pulse from the Logic Board to E6. This signal, amplified by transistors Q9 and Q8 and coupled through transformer T1, drives power transistor Q1. The amount of drive is modified somewhat by transistor Q10, which is controlled by the vertical parabola. Q10 thus causes the Q8 collector supply voltage (at T1-7) to be greater when the vertical sweep is at mid-point and lower when the vertical sweep is at top or bottom of the display. (This represents a part of the horizontal pincushion correction.) Q1 pulses fly-back transformer FBT1 through C71. (Note: In earlier models Q10 is omitted.)





Supply voltage for Q9 is +5V REF1 and for Q8 and Q10 it's the +15V unregulated. Both are referenced to frame ground.

The voltage and current to FBT1 is regulated by the circuitry including Q2, Q3, Q4, U1 and U4.

> CAUTION: Note that this is referenced to the 150V. "hot" common, not frame ground.

The unregulated 150V, connected through decoupling filter R17-C17, is regulated by power transistor Q2 to power FBT1. The remainder of the regulator circuit operates to control the conduction of Q2.

Two factors are involved in this control of Q2. One is negative feedback from (a) the Q2 emitter output through R9 to one input of U1 and from (b) the collector of Q4 through C13-C11-R15, also to U1 pin 3. Feedback from both sources is adjusted by HOR WIDTH potentiometer R109. The other factor is the vertical parabola signal through optical coupler U4, with adjustment by HOR PINCUSHION potentiometer R108. The signal from R108 is applied through R12 to the other input of U1. (This is the remainder of the horizontal pincushion correction, omitted from earlier models.)

The LED portion of the optical coupler has +5V REF1, referenced to frame ground, as its supply voltage. However, the photo transistor portion of U4 uses 3.9V REF 2, referenced to the 150V "hot" common. The supply voltages for U1 also are referenced to the 150V common.

The output of U1 is amplified by transistors Q4 and Q3 to control the conduction of Q2. Direct coupling is used. The collector supply for Q4 and Q3 is the unregulated 150V., reduced to approximately 140V. by R17, again with reference to the "hot" common, not frame ground.

FBT1, with current through Q2 and pulsed by Q1, generates the horizontal sweep current for the deflection coil in the CRT yoke assembly.

High Voltage DC, at two levels, is obtained by rectifying parts of the horizontal sweep waveform. From a separate winding of FBT1, the high voltage fly-back pulse is rectified to obtain approximately +20KV for the CRT anode. The rectifier and a voltage divider are in a sealed unit attached to the Analog Board near FBT1. One high voltage lead from this sealed unit has a connector for the CRT anode. Another high voltage lead from this sealed unit is terminated so as to mate with the Focus lead from the Video Board. The focus voltage is obtained from a voltage divider in the high voltage unit. The fine Focus adjustment is mounted on the Analog Board frame and is accessible through a hole in the cabinet rear cover.

Another portion of the horizontal wave form from terminal 1 of FBT1 is coupled through capacitor C30 to a rectifier and filter. The resulting DC voltage, approximately +200V referenced to frame ground, is used for CRT screen control in the Video Board.

Connections to the Analog Board from the yoke are through pins, mounted on the board, and connectorized twisted lead cable. Connections from the

Analog Board to other units are by twisted lead cables originating in the Analog Board and terminated in connectors for easy mating with connectors in other units. There are two ground clips.

E1-E6	To Logic Board (Sweep and convergence sync pulses)
E7-E10	To Power Board (Unregulated DC, 60 Hz. Sync)
E15-E18	To Video Board (DC voltages)
E19-E25	To Logic Board (Regulated DC voltages)
J1	To Yoke Assembly (Vertical Sweep and Convergence)
J2	To Yoke Assembly (Horizontal Sweep)

E. VIDEO BOARD

The Video Driver Board is mounted at the rear of the CRT by mating its socket to the CRT pins. It contains the three video drivers, three bias adjustment potentiometers and the socket for connections to the CRT. The circuit is shown on Schematic Drawing 100896.

Video Amplifiers are driven by signals from the Logic Board connected through J2. The signals for red, green and blue are passed through 74S37 gates UA1 to three identical driver transistors Q1, Q2 and Q3 (Q4, Q1 and Q7 in older boards). At the gate inputs resistors R19, R20 and R21 and diodes CR8 through CR13 help prevent transients resulting from CRT arcing from passing back to the Logic Board. The second input of the three gates is +5V. The 4th gate in UA1 is not used. Power for the gates is +5V regulated from the Analog Board, connected to UA1 terminal 14. A 1N4735 zener diode prevents the +5V supply from exceeding 6.2volts in case of regulator failure.

In the Red Drive circuit, transistor Q1 is a common-base amplifier. Its emitter is driven by the signal from UA1-3. The emitter bias is from the +5V Regulated and the collector supply from the -48V Regulated on the Analog Board, both connected through J1. The collector load includes frequency compensation to obtain the required bandwidth. Diodes CR1 and CR3 reduce the effect of CRT arcing. The Green and Blue circuits are similar. The driver outputs are connected through 1000-ohm series resistors (470 ohms in older units) and socket S1 to the CRT Red, Green and Blue control grids.

Screen Control Potentiometers R1, R2 and R3 provide individual bias adjustment for the Red, Green and Blue CRT Screen grids to control brightness and color mix. +200 VDC is supplied to three potentiometers via J1 from a rectifier associated with the horizontal sweep portion of the Analog Board.

6.3 VAC for the CRT socket filament connections is from transformer T1 on the Power Board, connected through J1.

Focus voltage for pin 9 of the CRT socket comes through a separate HV lead with a connector to mate with the Focus lead of the HV Rectifier(åttached to the Analog Board).

Cathode return for all three guns is to ground through R6 (10K).

Grounding connection for CRT socket terminal 10 and the tube mounting springs is to frame ground.

A typical video waveform at the collector of Q1 has an amplitude of approximately 40 volts p-p. The waveforms at UA-1, UA1-3 and Q1-e are approximately 4 volts p-p.

F. DISK DRIVE

The Floppy Disk Drive uses the standard 5 1/4" diskette package. Each of 40 tracks used for data(ôf 41 total tracks) is treated as consisting of 10 sectors with 128 bytes each--about 1280 bytes per track, including formatting information, or 51,200 bytes per diskette. The home "zero" track (outer most track) is not used for data. Compucolor II has provision for use of two floppy disk drives. The basic set includes one drive mounted in the right front of the cabinet. An optional external second disk drive can be connected to a branched Keyboard cable.

Modification Notes — Analog

The analog circuit description was for the board used in the frist several hundred units. A later board introduced certain changes outlined on a following page.

Still later, a few other changes were made.

1) The vertical ramp input was changed from DC to AC coupling. This first was done by insertion of two electrolytic capacitors, as described on a following page. Later a TL081 was inserted, as shown on 100902 Rev.7, to provide a high impedance load for a smaller coupling capacitor. The TL081 UA13 provided no voltage gain.

2) The power supply switching frequency was synchronized to the horizontal sweep rate to eliminate movement of noise lines in the display. Q10, shown between UA3 and UA4 on 100902 Rev.7, coupled a sync signal from the Logic board to both UA3 and UA4 through diodes CR32 and CR31.

3) The horizontal drive/high voltage switching transistor Q1 was changed from a BU500 to a BU157. An MJ12005 may be substituted if neither the BU500 nor BU157 is available.

4) In the horizontal voltage regulator, Q2 was changed from FT410 to 2SD348.

Modification Notes — Micro-Disk Drive

In the micro-disk drive controller board, R5 in series with the erase head went through a couple of changes. The final version used 100 ohms as R5. In units with a high value of resistance, compatibility problems between drives were not uncommon -- a disk recorded on one drive would not reproduce on another.

Also in the micro-disk drive controller board, R53 on the Rev.6 printed circuit board was relocated physically.

1) One end of an added 3300-ohm resistor is connected to the cathode end of CR1. The other end of the resistor is connected by an insulated lead to the feed-through hole to the lower left of R53 — the path from the left end of R53.

2) On the underside of the board, the path leadking from that feed-through hole is cut.

3) Still on the underside of the PCB, the left end of R53 is connected to the adjacent C30 lead.

The added 3300-ohm resistor now serves as R53. The old R53 on the PCB is shorted out.

Trouble-Shooting Note — Screen RAM

Occasionally a screen RAM IC with response a bit slow will cause spurious signals to appear on the screen, especially when scrolling. The following information may be of assistance in locating the problem IC.

Spurious Signal	IC Responsible
White block	UD11
White block with blink	UD10
Blue block, background blue	UD9
Zero (0), background green	UD8
Left bracket (, background red	UD7
Dollar symbol $, foreground blue	UD6
Quote marks ", foreground green	UD5
Exclamation !, foreground red	UD4

NOTES CONCERNING REVISED ANALOG BOARD

The Analog Board description contained in pages 5.03 through 5.15 covers the board used in the first several hundred production units. A redesigned board, introduced in 1979, has fewer parts and an improved component layout. The newer schematic is Rev.4; the newer PCB layout is Rev.3.

The basic functions of the board remain unchanged. The locations of the major circuit subdivisions on the schematic drawing are the same. However, there are a number of changes in components and component reference designations. This sheet outlines the major changes, many of which involve the convergence circuits.

1. A single DG300 IC (U5 on revised schematic) replaces Q12, Q13, Q14, Q15 and several associated components. The reset pulses, horizontal and vertical, now cause their respective sections of DG300 to operate for discharge of the ramp capacitors. (C83 is the horizontal ramp capacitor, C84 the vertical.)

2. Two sections of a TL084 IC (U6) replace two 741's for charging the ramp capacitors. Two other sections in the TL084 serve as comparators to generate square waves from the sawtooth ramps.

3. A DG303 (U7) replaces the 4016 bilateral switch. It requires only two comparators for switch operation instead of the four required by the 4016.

4. Only +8 and -8 regulated voltages are needed by these IC's. VR1 supplies the -8V. as before. VR2 supplies +8V. and replaces a voltage divider.

5. Generation of the parabola and pincushion waveforms is unchanged.

Other Changes:

6. In the horizontal voltage regulation circuit, the MC741 (U1) is supplied by its own rectifier rather than by a voltage divider (originally R48-R10). CR24, connected to a primary tap of T4, provides +20V. referenced to the 150-volt common.

7. In the horizontal pincushion circuits Q10 has been eliminated. All of the correction is applied to the horizontal voltage regulator via the optical coupler.

8. Q11, once considered for power supply sync, is no longer shown near the right-hand SG3524.

9. The NE540 IC's in the convergence and vertical sweep amplifier circuits are supplied with +12 volts rather than +11 volts. (Q17, Q18 and Q19 still use +11V.)

10. Vertical pincushion correction is fixed, eliminating one potentiometer.

11. Voltage limiting diodes have been added at the +5V. and +12V. rectifier outputs for circuit protection.

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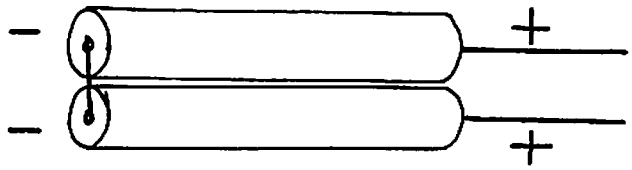
COMPUCOLOR II CIRCUIT CHANGE NOTES

In some cases you may find it desirable to make changes in early production units similar to those introduced during recent production.

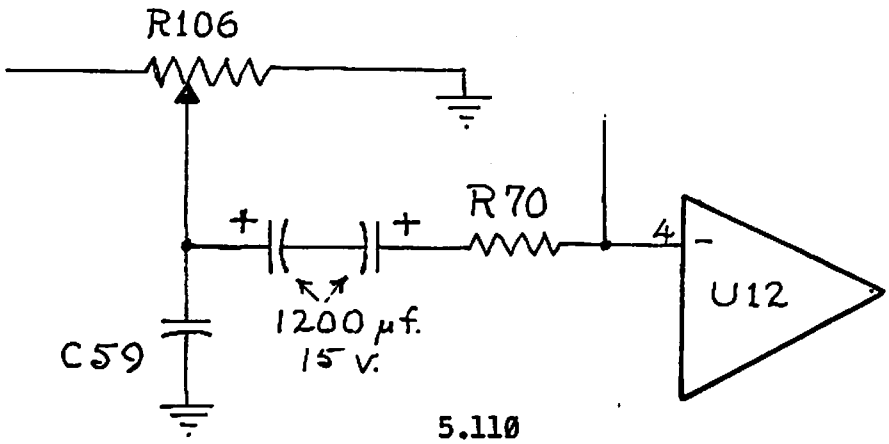
1. On the Analog Board series capacitors may be inserted in the vertical amplifier input. Occasional Logic Board hang-ups at turn-on prevent generation of ramp reset pulses. Such hang-up, or other failure of ramp reset pulse, may result in a blown F1 fuse in the vertical amplifier and damage to the parallel 100-ohm resistor R75 or resistors R50 or R51. Series capacitors are now being used between the vertical height potentiometer R106 and R70 to prevent this damage. This circuit change can be made to any of the earlier production units.

Disconnect the end of R70 nearest the Vertical Height potentiometer R106. Form R70 perpendicular to the board. Assemble and connect two 1200uf 15-volt capacitors as shown below.



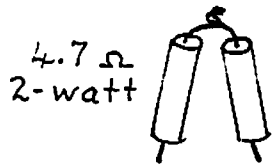
Tie-wrap them to the underside of the frame fold-over just above U13. Using short insulated leads, connect one capacitor positive lead to the free end of R70 and the other capacitor positive lead to the point from which one end of R70 was removed.

The circuit then becomes:



2. In the 150-volt input to the horizontal voltage regulator, 10-ohm resistor R17 has been changed to two 4.7-ohm, 2-watt resistors in series to provide greater heat dissipation margin. To make this change in the Analog Board:

Remove 10-ohm, 2-watt resistor R17. Connect two 4.7-ohm, 2-watt resistors as shown and connect in circuit as R17.



3. If addition of Horizontal Pincushion is deemed desirable in the case of early production units, the change may be made. Mount parts in the vacant PCE locations near the fly-back transformer and near the rear lower edge of the Analog Board.

POSITION	PARTS TO BE MOUNTED
U4	4N37 Optical Coupler
R34	820 ohms 1/4 watt
R38	2.2K 1/4 watt
R39	2.2K 1/4 watt
R12	47K 1/4 watt in series withh 0.1uf 12V.
C14	0.01uf 12V.
R108	20K potentiometer
R119	Replace with two 47K 2-watt resistors in parallel

With page erased in a color other than black, adjust R108 to obtain straight raster sides.

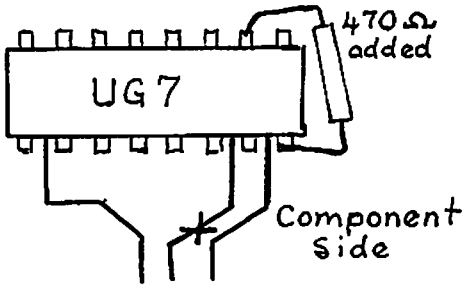
4. On the Power Board, varistors across the bridge rectifiers are useful in preventing voltage spike damage to other components.

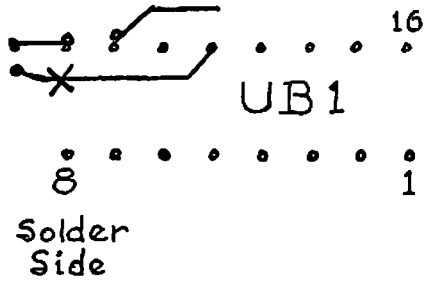
Connect a V130LA10A varistor in the mounting holes for C2 & C4 nearest the transformer.

Connect a 22Z1 varistor across bridge rectifier BR3 AC input terminals on the back of the board.

5. On the Logic Board, improved reliability in the operation of the 74LS163 Counter UG7 has resulted from insertion of a section of 74LS04 Inverter UC1 in UG7's clock input. To make this change in the Logic Board:

Cut the PCB circuit path between UB1 terminal 12 and UG7 terminal 2 in two places, one near UG7 and one near UB1.



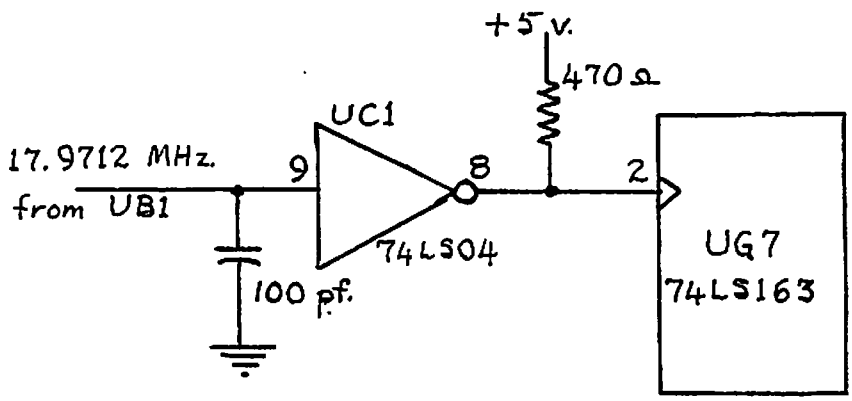


On the component side, connect a 470-ohm 1/4 watt resistor across terminals 2 and 16 of UG7.

Connect a 100pf 1KV disk capacitor across terminals 7 and 9 of UC1.

On the solder side of the board, connect insulated wire leads between UB1 terminal 12 and UC1 terminal 9 and between UC1 terminal 8 and UG7 terminal 2.

The circuit then becomes:



6. For any very early Video Drive Boards without the protective diodes, they may be added as follows:

On the component side of the board, mount 1N914 diodes in the CR1, CR2 and CR3 positions. (The cathode ends are toward the transistor collectors.)

On the solder side connect 1N914 diodes across the base and collector of the three transistors (cathode end to base of transistor).

Connect three 1N914 diodes on the solder side of J2. Anodes of all three connect to terminal 1. The three cathodes connect to terminals 3, 4 and 5.

Still on the solder side, connect the cathode ends of three 1N914 and one 1N4735A to terminal 14 of UA1. Connect the anode ends of the 1N914's to terminals 1, 4 and 13 of UA1. The anode end of the 1N4735A zener connects to the nearby ground lead (to which terminal 7 of UA1 is connected).

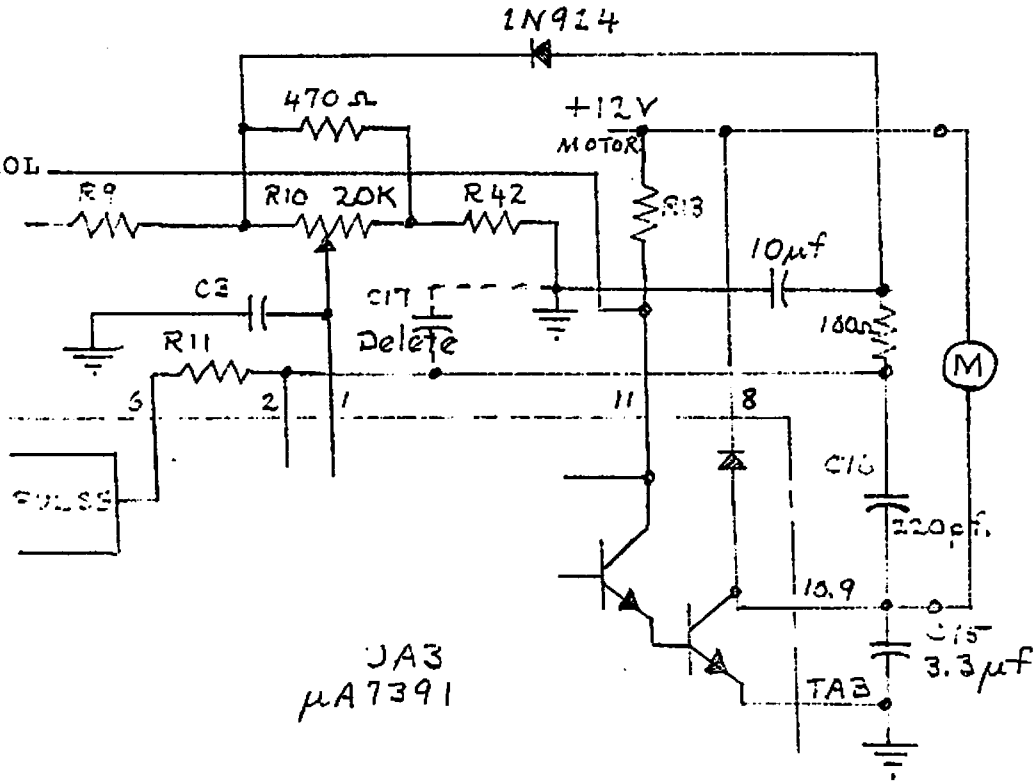
7. Most Disk Controller Boards having the original circuit have been modified to one of the improved versions. If you should have any unmodified unit which is causing problems, it can be modified. However, we suggest you contact your customer service representatives to arrange having this done by the factory.

COMPUCOLOR II MAINTENANCE MANUAL CHANGE NOTES

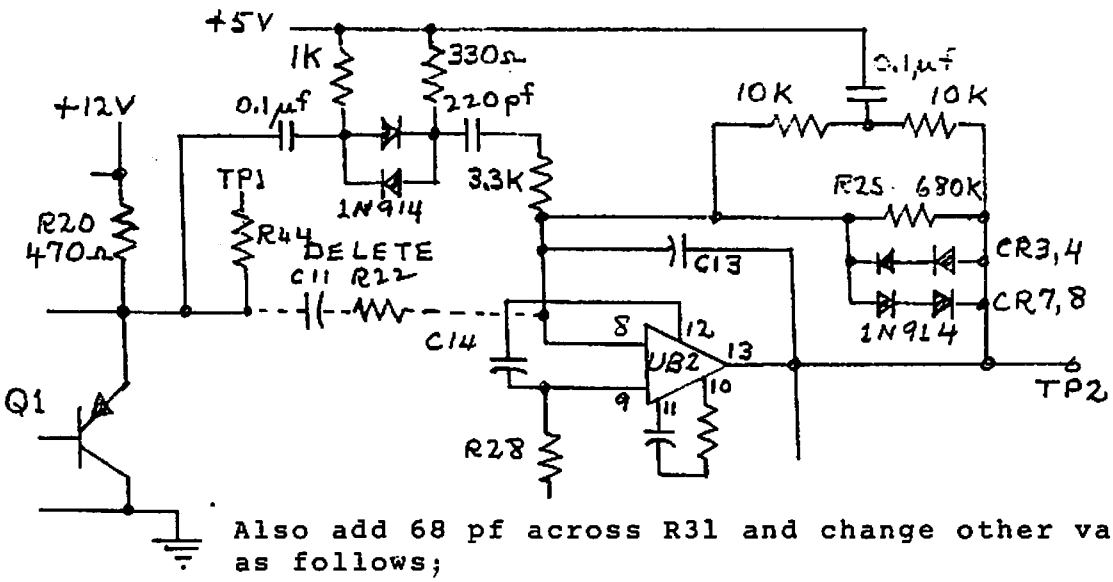
Reliability has been improved by a number of design changes currently in production. Revised drawings will be included in a manual up-date package to be issued in December or January.. In the meantime. you may wish to note the following information in your Maintenance Manual.

Disk Controller Schematic - changes in motor speed control circuit and reproduce amplifier circuit.

MOTOR CONTROL CIRCUIT



REPRODUCE AMPLIFIER

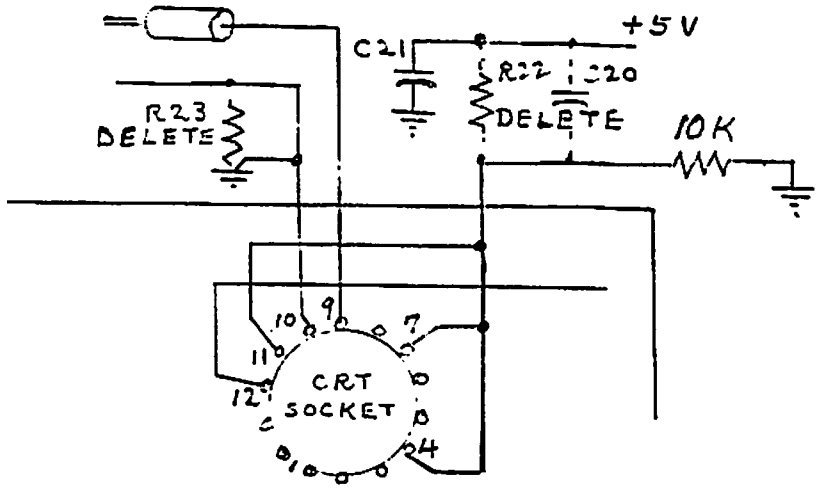


Also add 68 pf across R31 and change other values as follows;

C4	220pf.	R15,R16	1K	R24	470Ω
C8	470pf.	R17,R19	680K	R33	8.2K

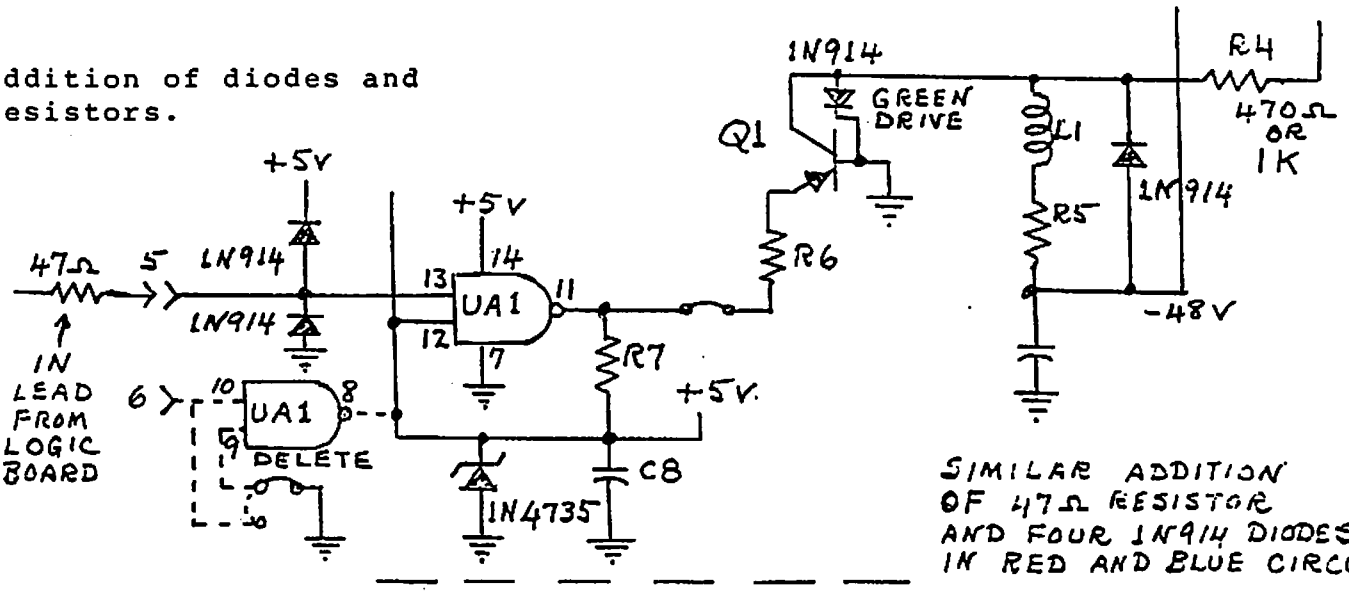
VIDEO DRIVER SCHEMATIC

Deletion of C20, R22 & R23



Changes in grounding

Addition of diodes and resistors.

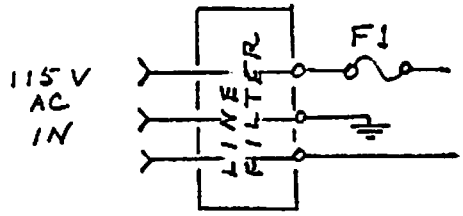


LOGIC BOARD SCHEMATIC

74LS123 section to right of 3242(UA3) should be UG4.

ANALOG SCHEMATIC

On Power Board show line filter.



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SECTION VI

MAINTENANCE

VI. MAINTENANCE

General

This section contains information useful in maintenance of a 3600-Series Intecolor unit. It includes preventive maintenance, safety and servicing precautions, instrumentation requirements and trouble-shooting suggestions. (Alignment procedures were described in Section IV.)

A thorough understanding of the circuit descriptive material is essential to effective corrective maintenance.

Safety Precautions

1. HAZARDOUS VOLTAGES are present within the unit. Exercise CAUTION especially to avoid contact with the CRT high voltages, the input 115 VAC (or 220 VAC) and the +300 VDC circuits.

2. Do not remove, install or handle the cathode ray tube in any manner unless shatterproof goggles are worn. Persons not so equipped should be kept away while the CRT is being handled. Keep the CRT away from the body while handling.

3. Always use the manufacturer's recommended replacement components when replacing parts, especially in the Analog Module circuits associated with the cathode ray tube. Use of the correct parts is an essential step in keeping X-radiation at a minimum.

4. When service is required, observe the original lead dress. Extra care should be taken to assure correct lead dress in the high voltage circuitry and the video area.

5. Where a short circuit has occurred, replace those components that show evidence of overheating.

6. REMEMBER that part of the Analog CIRCUITRY is NOT REFERENCED TO FRAME GROUND. When making measurements or viewing waveforms in circuits associated with the +300V supply, one of the following procedures must be used:

a. Any instrumentation connected to this part of the circuit must be isolated from frame ground.

b. Or the Intecolor unit itself must be "floated" by use of an isolation transformer between the Intecolor unit and the AC supply.

Preventive Maintenance

The 3600-Series Intecolor unit requires a minimum of preventive maintenance: periodic cleaning and visual check of the interunit cabling and the chassis components; occasional touch-up of convergence adjustments. To clean the CRT screen, use a lightly moistened lint-free cloth or a vacuum cleaner. Use a vacuum cleaner to clean the Analog Module and other components.

Servicing Precautions

Several precautions to be observed while servicing the solid state chassis are listed below:

1. Always connect the ground (or common) lead of a test instrument to the chassis (or common point) before connecting the positive (or signal) lead; conversely, always remove the ground or common lead of a test instrument last.

2. Do not check for high voltage by drawing an arc. Use a high voltage meter or a high voltage probe with a VOM.

3. Do not bridge electrolytic capacitors into a live circuit -- the resulting surges may damage solid state devices.

4. Some transistors are equipped with heat sinks. Do not operate the transistor with the heat sink removed.

5. All soldering irons used where transistors and integrated circuit chips are concerned should be 35 watt (6 volts) irons and ungrounded so that no voltages will be applied to the solid state device during the soldering operation. This precaution is for prevention of possible damage to the device by excessive heat or voltage applied under no-bias conditions.

Instrumentation

Performance of complete alignment procedures requires use of an oscilloscope with a bandwidth of 15 MHz. and an accurate VOM -- preferably a digital VOM for adjusting the +5 VDC supply. For measuring the CRT high voltage, the VOM must have a high voltage probe or a separate high voltage meter must be used (up to 25 KV). (Remember to "float" the oscilloscope and any electronic VOM before connecting to certain circuits!) Use of a multiple trace oscilloscope often is desirable.

For trouble-shooting in the video area and portions of the digital area a considerably wider bandwidth oscilloscope is needed -- 100 MHz. bandwidth is recommended. A digital logic probe can be useful.

CABINET DISASSEMBLY

The 3600-Series Intecolor must be partially disassembled for most alignment and trouble-shooting. The line fuse, the high voltage circuit fuse and the focus and brightness controls are readily accessible at the rear of the console. The nine-sector convergence controls are accessible at the front by removal of a snap-off cover. Connectors for peripheral equipment are accessible at the rear. However, access to all other controls and components calls for removal of the top and/or rear cover.

Power should be off when interunit cables are disconnected.

Top Cover -- Removal of the top cover is necessary for most trouble-shooting and adjustment work. At the front edge of the console, just below the keyboard, remove two screws from the front. Lift the cover by the front edge and tilt the cover approximately 45°. Gently slide the cover forward a bit to clear the rear edge from its holding area and lift off the cover. The alignment and adjustment controls are now accessible and most connectors as well. The rear cover protects the technician from accidental contact with the voltage on the collectors of the power transistors.

Rear Cover -- Removal of the rear cover is required for access to the power transistors and for removal of the Analog Module and Video Assembly. Along the top edge of the rear cover, remove three screws. Rotate the top edge of the rear cover to the rear. Lift the lower edge slightly to clear the holding tabs and remove the cover to the rear. CAUTION: WHEN POWER IS ON, HAZARDOUS VOLTAGES ON THE TRANSISTOR COLLECTORS ARE EXPOSED.

Analog Module -- First remove the top and rear covers from the console. Next, cables to the Analog Module should be disconnected before removal of the module. (However, the cables may be left connected when merely moving the module back a bit to permit removal of the Video Assembly.) Disconnect the power cord from its socket on the module rear panel and the high voltage lead from the CRT. Disconnect the power and sync cables from the Digital Module -- these are accessible through the rectangular opening in the Analog Module. Disconnect two connectors from the Video Assembly and the connectors from the CRT yoke (for horizontal sweep, vertical sweep and convergence). Along the upper edge of the module rear panel, remove three mounting screws. Slide the module to the rear a bit to clear the slots that hold the module front edge in place. Now the module may be lifted slightly to allow the video cable to be disconnected from the Digital Module. Carefully remove the Analog Module toward the rear.

Video Assembly -- First remove the top and rear covers from the console. On the Video Assembly board, disconnect two Analog Module cable connectors. Disconnect the focus voltage lead and then the yellow grounding strap. On the Analog Module, remove the three mounting screws (upper edge of module rear panel) and move the Analog Module a couple of inches to the rear. The Video Assembly now may be removed from the CRT.

Digital Module -- The Digital Module may be removed with the console rear cover in place. First remove the top cover. Then disconnect any edge connectors from the rear edge of the printed circuit board. Disconnect the power and sync cables (accessible through the rectangular opening in the Analog Module). Near the center of the Digital Module rear edge, remove the single holding screw and bracket. Slip the board an inch or two to the rear. Disconnect the video cable (accessible now through the opening in

the Analog Module) and the Disk Drive cable (use care to avoid bending the connector pins -- a small screwdriver helps to free the connector ends a little at a time). Slide the Digital Module out to the rear.

Disk Drive -- Remove the top cover from the console. Then carefully disconnect the flat flexible cable from the disk controller board -- a small screwdriver helps free the connector ends a bit at a time to avoid bending the connector pins and possible injury to one's fingers. The two screws holding the disk drive assembly in place are accessible from the under side of the console pan. Support the disk drive when removing the second screw.

Keyboard Assembly -- Remove the console top cover. Then remove the edge connector from the rear edge of the keyboard printed circuit board. Note that the keyboard assembly is keyed in position at slots in both ends and is held in place by two round slotted posts. The left post (left, as viewed from the front) can be bent away from the keyboard frame enough to allow the left end of the keyboard assembly to be lifted upward. From the bottom of the console, insert a long-handled tool such as a #2 Phillips screwdriver through the bottom pan hole adjacent to the left post. Use leverage to bend the post outward and lift the left end of the keyboard assembly clear. Then the assembly can be slipped to the left to clear the other hold-down slot.

Convergence Assemby -- Remove the console top cover and then the Disk Drive Assembly. Two screws hold the inside edge of the printed circuit board in place. Remove these and lift the assembly away to the rear. For complete removal, carefully disconnect the flat flexible cable -- care is required to prevent bending the connector pins and injury to one's fingers.

Trouble Shooting Techniques

Some of the items listed below seem fairly obvious, but sometimes they are overlooked.

1. Check to see that all plugs and connectors are properly connected.

2. Check for blown fuses.

3. Make a visual check for broken connections and damaged components.

4. If there is a convergence problem, first try correcting it by alignment -- see Section IV Alignment for the procedure.

5. Always check the low voltage power supplies -- this usually should be one of the first items in trouble-shooting.

6. Verify that sync and video signals are input to the Analog Module.

7. Note symptoms and refer to the symptoms chart.

8. Locate the circuit area in which the problem is believed to exist.

9. Review the circuit description of the suspected circuit.

10. Where possible, follow a signal-tracing procedure through the circuit until the faulty area and component(s) are found.

11. The power transistors mounted on the Analog Module frame can be removed fairly easily for check with an ohmmeter or a transistor tester.

12. Exercise care in removing suspected components to avoid damage to the conducting areas on the printed circuit boards -- and to permit reuse of the component in case it should prove good!

13. When spare modules are available, substitution for a suspect module is very helpful is isolating the problem to a specific module.

SYMPTOMS CHART

Observed Symptom	Circuit Description Section
Loss of high voltage	Pages 5.20 through 5.25. In the Analog Module, check F2; check for horizontal drive pulse at J5-1.
Loss of low voltages	Pages 5.03 - 5.09. Check F3.
Loss of low voltage regulation	Pages 5.03 - 5.09.
Loss of video	Pages 5.25 and 5.27. Verify that it's not a case of lost high voltage.
Horizontal jitter	Pages 5.20 - 5.24. Check horizontal position adjustment.
Loss of convergence control, right and left screen area	Pages 5.10 - 5.12. Check for horizontal reset pulse at J5-2.
Loss of convergence control, top and bottom screen area	Pages 5.13 - 5.14.
Loss of convergence control, corner areas	Pages 5.15 - 5.18.
Total loss of convergence, one or more colors	Page 5.18

INTERCONNECTIONS

From	To	Description
Convergence Bd J1	Analog Module J12	Convergence waveforms
Video Assembly J1	Analog Module J3	DC and AC Power
" J2	" J1	Video signals
" Lead	" Lead	Focus voltage
" Tab	Frame yellow strap	Ground
Internal Disk J1	Digital Module J7	Data, control, power
Digital Module J1	Keyboard	Data, DC power
" J2	RS-232C Port socket	Serial data
" J3	User designation	50-Pin Bus
" J4	Analog Module J4	Video signals
" J5	" J5	Sync signals
" J6	" J6	DC power
" J7	Internal Disk J1	Data, control, power
Analog Module J1	Video Assembly J2	Video for display
" J2		Future use
" J3	Video Assembly J1	DC and AC Power
" J4	Digital Module J4	Video signals
" J5	" J5	Sync signals
" J6	" J6	DC power
" J7		Future use
" J8	CRT Yoke	Vertical deflection
" J9	"	Convergence
" J12	Convergence Bd J1	Convergence waveforms
" J13	CRT Yoke	Horizontal deflection
" white lead	Video Assembly Lead	Focus voltage
" red lead	CRT Anode	CRT high voltage

Note: Early production Analog Modules have three connectors for the convergence waveforms to the CRT Yoke -- J9 for Blue, J10 for Green and J11 for Red.

COMPUCOLOR II MAINTENANCE NOTES

General

This section contains information required for maintenance of the Compucolor II. It covers preventive maintenance, adjustment procedures, trouble-shooting sugguestions and parts replacement instructions.

A thorough understanding of the system and sub-assembly descriptive material, including the drawings, is essential for effective maintenance.

Safety Precautions

1. HAZARDOUS VOLTAGES are present within the Compucolor II. When the rear cover is removed for adjustments and/or trouble-shooting, exercise CAUTION especially to AVOID CONTACT WITH THE CRT HIGH VOLTAGES, THE INPUT 115 VAC, AND NUMEROUS CIRCUITS IN THE POWER, ANALOG AND VIDEO BOARDS HAVING 150 VDC AND HIGHER.

2. Do not remove, install or handle the picture tube in any manner unless shatterproof goggles are worn. Persons not so equipped should be kept away while picture tubes are being handled. Keep the picture tube away from the body while handling.

3. Always use the manufacturer's recommended replacement components when replacing parts, especially in the Analog Board circuits associated with the cathode ray tube. Use of the correct parts is an essential step in keeping X-Radiation at a minimum.

   The only source of X-Radiation in the Compucolor II is the picture tube. The cathode ray tube used is specifically constructed to limit X-Radiation. For continued X-Radiation protection, the replacement tube must be the same type as the original, including suffix letter, or a Compucolor Corporation approved type.

   The CRT high voltage must be maintained within specified limits. The high voltage must never, under any circumstances, exceed 25 KV. The usual value is near 20 KV.

4. A further caution:

   Part of the Compucolor II circuitry on the Power and Analog Boards is not referenced directly to frame ground. The rectifier for 150 VDC is connected to the 115VAC line, so the 150-volt supply and all circuits directly supplied by it have a "hot" common lead, several volts from frame ground. Any instrumentation to be connected across these circuits must be floating --- neither side grounded.

Cabinet Disassembly

The Compucolor II cabinet must be partially disassembled for most alignment and trouble-shooting. Care must be exercised to avoid damage to the Logic Board and Video Board during removal of the rear cover. With power off, disconnect the keyboard and any external additions connected to the rear edge of the Logic Board.

Remove the four screws (3 top, 1 bottom) that fasten the rear cover to the front portion of the cabinet. Then, with the cabinet upright on the bench, slide the rear section back slowly to allow the Logic Board to drop gently from its retaining slots in the front and rear sections. This procedure also avoids rear cover contact with the Video Board mounted on the back of the cathode ray tube. The keyboard now may be reconnected and power applied to the unit. Normal alignment procedures require no further disassembly.

Trouble-shooting and/or repair likely will require further disassembly. Power should be off when interunit cables are to be disconnected.

Video Board - Circuit measurement points are readily accessible with the board in place. If component replacement or other repair is indicated, disconnect the cables to the Analog and Digital Boards; carefully disengage the Video Board from the CRT.

Analog Board - Measurements required during alignment may be performed with the Analog Board in place. Further access likely will be required during trouble-shooting. Remove three mounting screws (one bottom, one at lower left and well into the forward section of the cabinet, and one at the top). Then the unit can be moved enough to make its components somewhat more accessible. For complete removal, first disconnect all cables to and from the board.

Power Board - Disconnect the power cord and the internal cable to the Analog Board. Remove two mounting screws from the exterior side of the rear cover.

Disk Drive - Disconnect the cable from the Logic Board. The unit is fairly heavy relative to its small size. It should be supported by hand carefully to avoid damage to the circuit board during removal. Remove the Phillips head screw from the bracket strip just above the drive assembly, as viewed from the rear. Tilt the rear of the drive unit up a bit and lift the entire assembly slightly to free the two tabs securing the lower front of the drive assembly. Remove the Disk Drive through the front of the cabinet.

Operational Test

Within one minute after unit is turned on, the first line of the screen display should be "DISK BASIC 8001 V6.78 COPYRIGHT © BY COMPUCOLOR", in colors against a black background. (Note: It may be necessary to strike the CPU RESET key once or twice).

Erase the screen with the background color Red.

1) Operate the "BG ON" key.
2) With "CONTROL" key depressed, strike the red "Q" key.
3) Operate the "ERASE PAGE" key.

There should be a uniformly red raster a bit larger than 6" x 9" centered on the screen. The top and bottom edges of the display should be straight. The cursor should appear in the upper left corner of the display.

In similar fashion check the colors Green ("R" key), Yellow ("S"), Blue ("T"), Magenta ("U"), Cyan ("V") and finally Black ("P"). (With the screen erased in Black there is, of course, no visible raster. Only the cursor appears).

Fill the screen with a pattern of white letters.

1) Strike the "FG ON" key.
2) With "CONTROL" key depressed, operate the White "W" key.
3) Strike the "(ESC)", "Y" and "T" keys in succession.

The full-screen pattern of letters should be uniformly White.

Operate the "CPU RESET" key. The pattern of letters is erased and the screen displays "COMPUCOLOR II CRT MODE V6.78". The cursor is at the start of the second line.

Verify that the "CAPS LOCK" key is in the depressed position. Then type material using all keys, for example:

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG'S BACK.(Space) 1234567890.(Space)

[\]^_(TAB)-(TAB)@;:,/(TAB)<?> +*(TAB)NULL!"#$(TAB)%&(=)

(Note: In order to check both "SHIFT" keys, use the right hand key for some characters and the left hand "SHIFT" key for the others).

Depress "REPEAT" and "." keys simultaneously to add 6 or 8 dots. The line of symbols should read:

[\]^_ - @;:,/ <?> +* ■!"#$ %&(=).....

Verify that the cursor is near the end of the line of symbols. Strike the "ERASE LINE" key. The line of symbols should be erased and the cursor should return to the start of that line.

Operate the "HOME" key. The cursor returns to the upper left corner of the screen. Operate the other cursor control keys to verify that the cursor moves down, right, left and up in accordance with the direction key operated. End with the cursor down a few lines from any material already displayed.

Strike the "A7 ON" key, then the "BLINK ON" key. Then type

BLINK (BL/A7 OFF) TEST

The word "BLINK" is displayed in double height letters and blinks on and off almost two times per second. "TEST" is in normal height letters and does not blink. (Note: In Models 1 and 2, all letters are the same height).

With both "SHIFT" and "CONTROL" keys held down, operate the "CPU RESET" key. The "DISK BASIC" message should appear. Insert the sampler diskette into the disk drive and close door. (See page 2 of the "Instruction Manual"). Depress "AUTO" key. The disk drive runs. A "MENU" or program listing appears on the screen. Strike the "5" key and then the "RETURN ENTER" key. The Compucolor II runs through a memory test, displays "TESTED OK" and then a series of graphic displays follows.

The above test procedure verifies operation of all keys on the standard keyboard and provides a fairly comprehensive test of computer and display functions. Intermittent failures and certain specific problems may require additional testing. Overnight operation prior to final test is recommended.

SECTION VII

PARTS LIST

VII. PARTS LIST

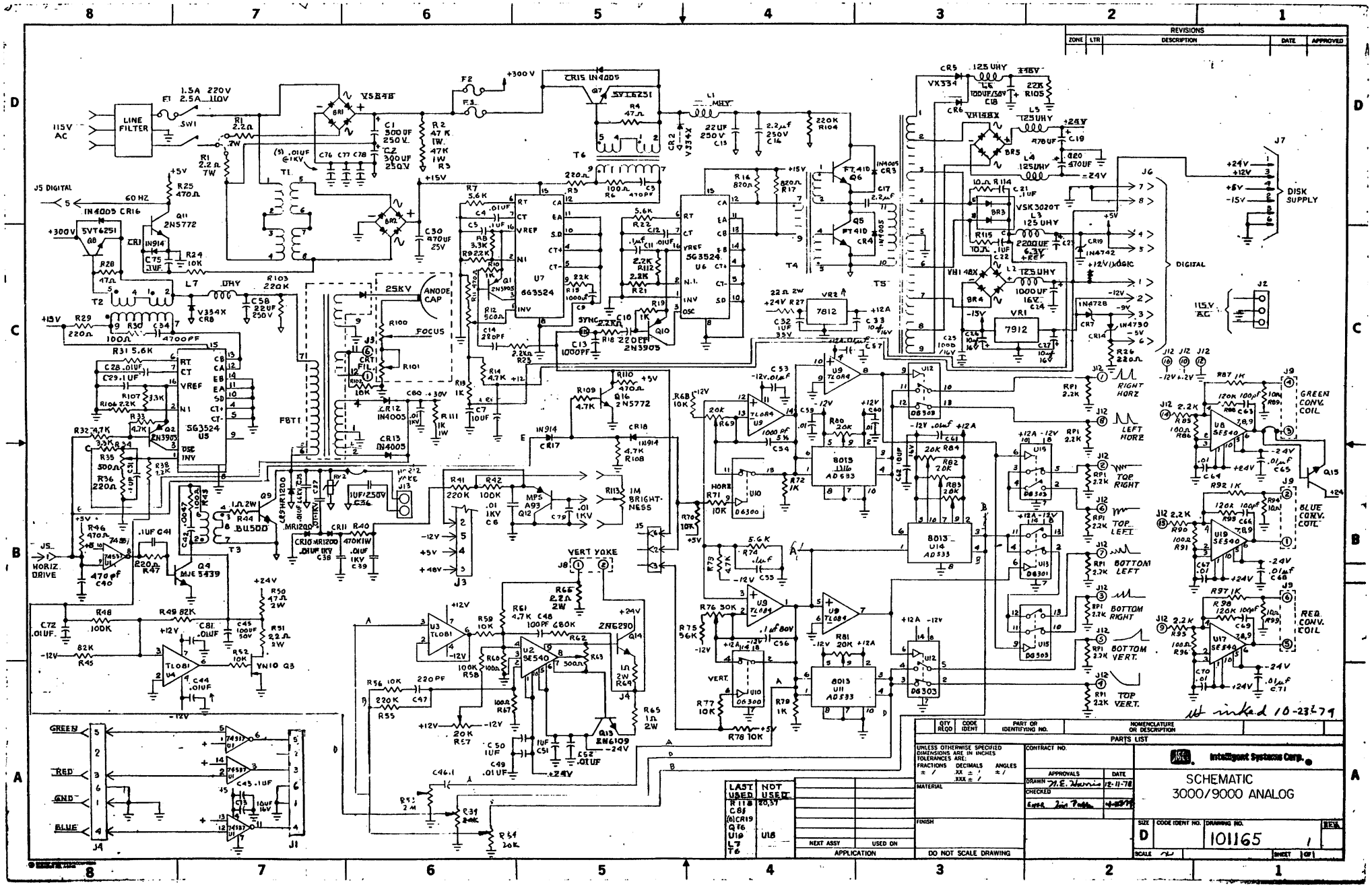
Description	ISC Part Number
Analog Module Assembly	101167
Convergence Assembly	101164
Video Driver Assembly	101176
Logic Assembly - No User RAM	101279
Logic Assembly - 16K	101259
Logic Assembly - 32K	101261
Add-On RAM Assembly - 16K	100986
Add-On RAM Assembly - 128 Byte	101045
Micro Disk Drive Assembly	101220
PCB Assembly only for Disk Drive	100872
Keyboard Assembly - 72 Keys	101225
Keyboard Assembly - 101 Keys	101226
Keyboard Assembly - 117 Keys	101227
Spare Parts Kit - Analog Module	0099B0
Spare Parts Kit - Digital Module	010048
CRT 13" - 370AJB22	900002

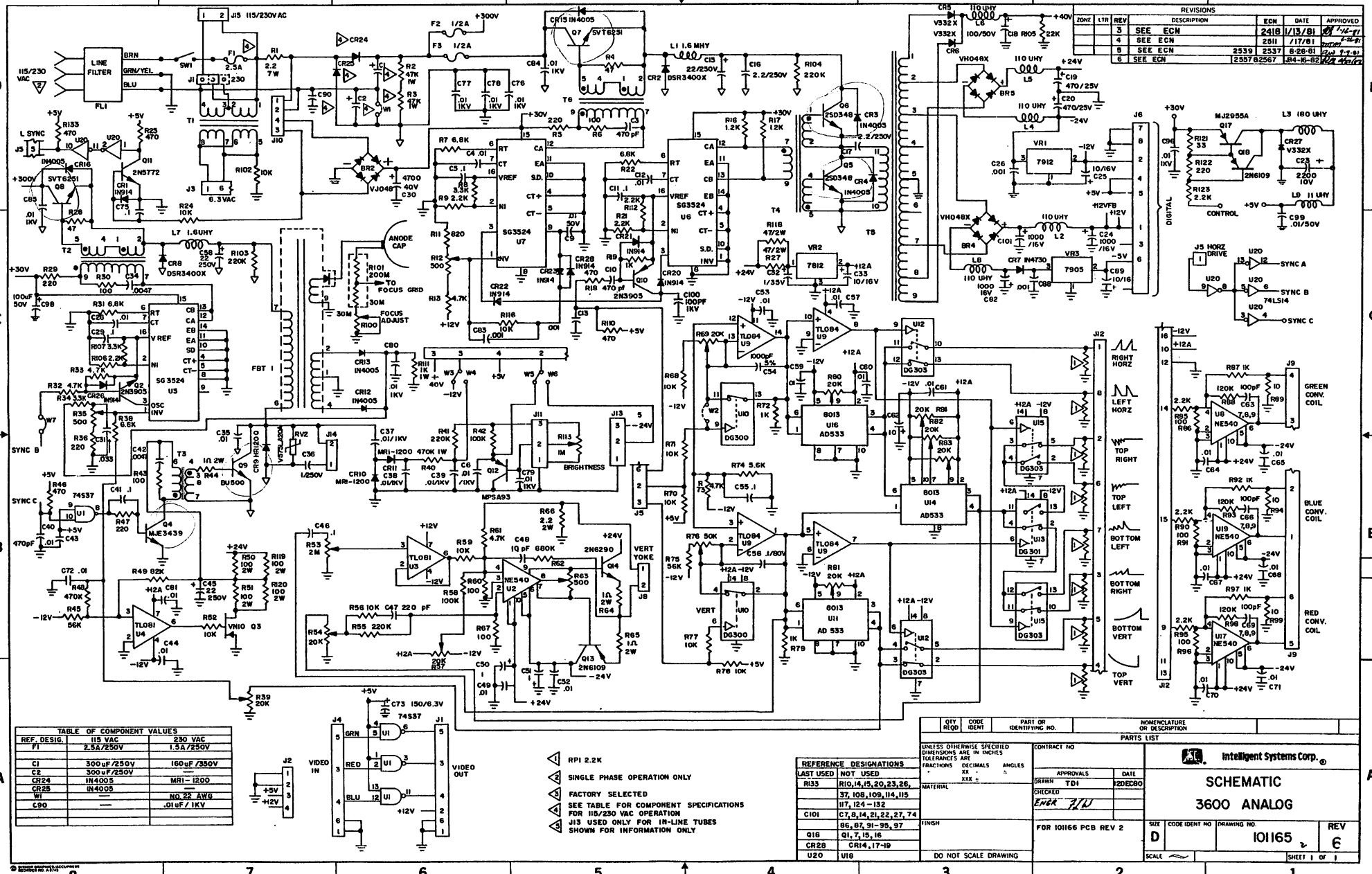
The above list shows major subassemblies only. For repair of subassemblies, Intelligent Systems Corporation can supply parts not commonly available from electronics supply houses. The minimum order total for such parts ordinarily is $100.00.

NOTE: The above part numbers continue to be shown for reference only. Please discuss possible substitutions with Intecolor applications engineers prior to ordering. Address and telephone number are shown on the title page of this manual.

SECTION VIII

DRAWINGS


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
LINE FILTER
115V AC
SW1
F1 1.5A 220V
F2
F3
+300V
+15V
+5V
+24V
-12V
-24V
SG3524
SG3524 U5
SG3524 U6
SG3524 U7
TL084
TL081
SE540
AD533
DG303
DG300
DG301
DG309
7812
7912
DISK SUPPLY
DIGITAL
ANODE CAP
FOCUS
CRT1
VERT YOKE
HORIZ. DRIVE
RIGHT HORZ
LEFT HORZ
TOP RIGHT
TOP LEFT
BOTTOM LEFT
BOTTOM RIGHT
BOTTOM VERT.
TOP VERT.
GREEN CONV. COIL
BLUE CONV. COIL
RED CONV. COIL
BRIGHTNESS
GREEN
RED
GND
BLUE
J1
J4
J5 DIGITAL
60 HZ
Intelligent Systems Corp.
SCHEMATIC
3000/9000 ANALOG
DRAWING NO. 101165
SIZE D
SCALE 1/2
SHEET 1 OF 1
DRAWN M.E. Harris 12-11-78
PARTS LIST
DO NOT SCALE DRAWING
linked 10-23-79


REVISIONS
ZONE | LTR | REV | DESCRIPTION | ECN | DATE | APPROVED
3 | SEE ECN | 2418 | 1/13/81
4 | SEE ECN | 2511 | /17/81
5 | SEE ECN | 2539 | 2537 | 6-26-81
6 | SEE ECN | 2557 | 2567 | 8-6-82
TABLE OF COMPONENT VALUES
REF. DESIG. | 115 VAC | 230 VAC
FI | 2.5A/250V | 1.5A/250V
C1 | 300uF/250V | 160uF/350V
C2 | 300uF/250V | —
CR24 | IN4005 | MRI-1200
CR25 | IN4005 | —
WI | — | NO.22 AWG
C90 | — | .01uF/1KV
RPI 2.2K
SINGLE PHASE OPERATION ONLY
FACTORY SELECTED
SEE TABLE FOR COMPONENT SPECIFICATIONS FOR 115/230 VAC OPERATION
J13 USED ONLY FOR IN-LINE TUBES SHOWN FOR INFORMATION ONLY
REFERENCE DESIGNATIONS
LAST USED | NOT USED
R133 | R10,14,15,20,23,26, 37, 108, 109, 114, 115
C101 | C7,8,14,21,22,27,74 86,87,91-95,97
Q18 | Q1,7,15,16
CR28 | CR14,17-19
U20 | U18
PARTS LIST
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS | DATE
DRAWN TDI | 12DEC80
CHECKED ENGR
FOR 101166 PCB REV 2
Intelligent Systems Corp.
SCHEMATIC
3600 ANALOG
SIZE D | CODE IDENT NO | DRAWING NO. 101165 | REV 6
SCALE | SHEET 1 OF 1

6-7-8-9

2SD342

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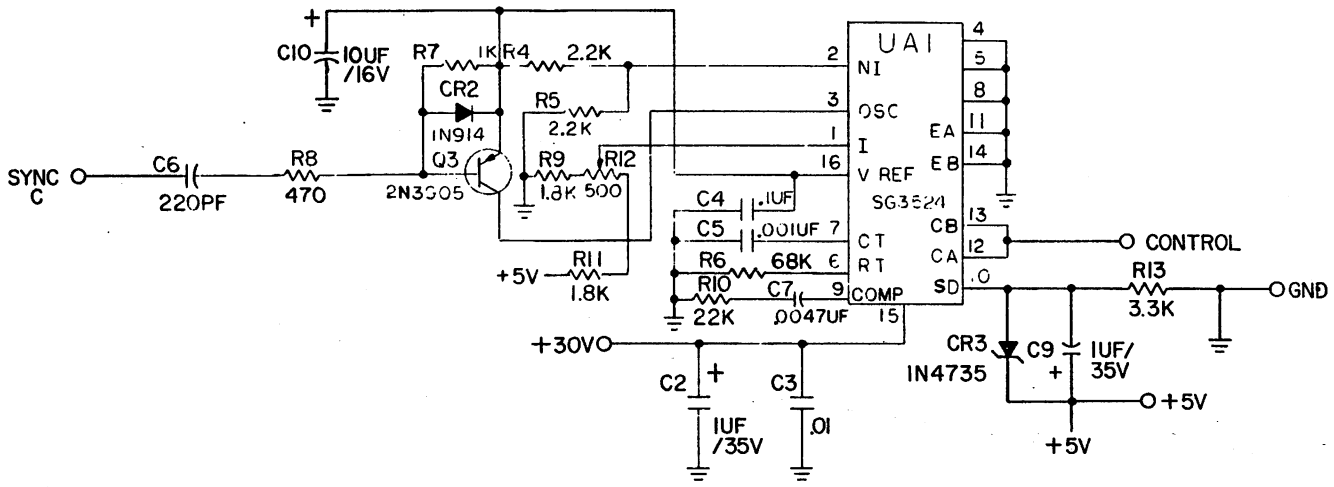


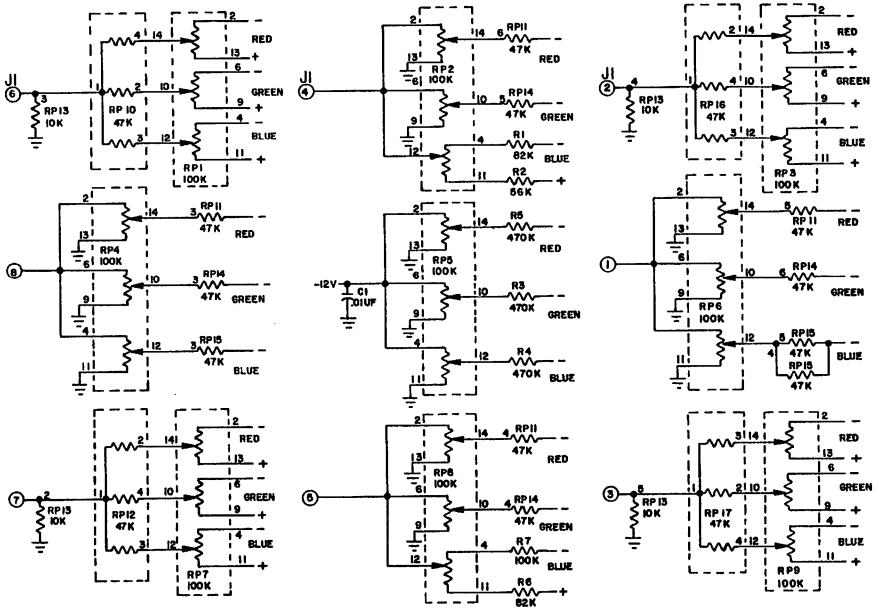
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	Intelligent Systems Corp. ®	
MATERIAL	APPROVALS / DRAWN / CHECKED / ENGR	DATE / 12-17-80	SCHEMATIC ANALOG 5 VOLT POWER SUPPLY
FINISH	SIZE C	DRAWING NO. 101682	REV. 1
DO NOT SCALE DRAWING	SCALE ~	SHEET 1 OF 1	

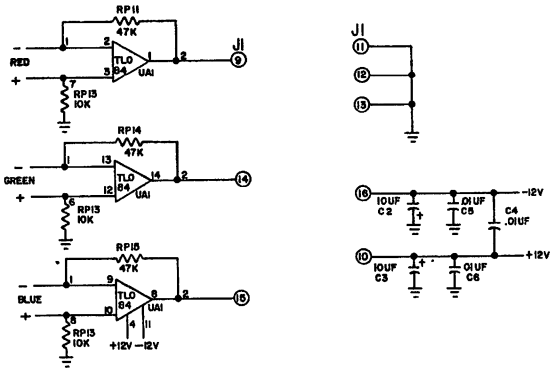
REV	LTR	REVISIONS DESCRIPTION	ECN	DATE	APPROVED
1		ENGR. RELEASE	2097	10/11/79 DS	
2		CHG DRWG TITLE	2583	12/9/81 NH	

TOP LEFT CORNER

TOP CENTER

TOP RIGHT CORNER





LAST USED	NOT USED
R7	
RP17	
C6	
J1	
NEXT ASSY	USED ON
APPLICATION	

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX
XXX

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN Duane Snyder	10-10-79
CHECKED	

FOR REV-I PCB

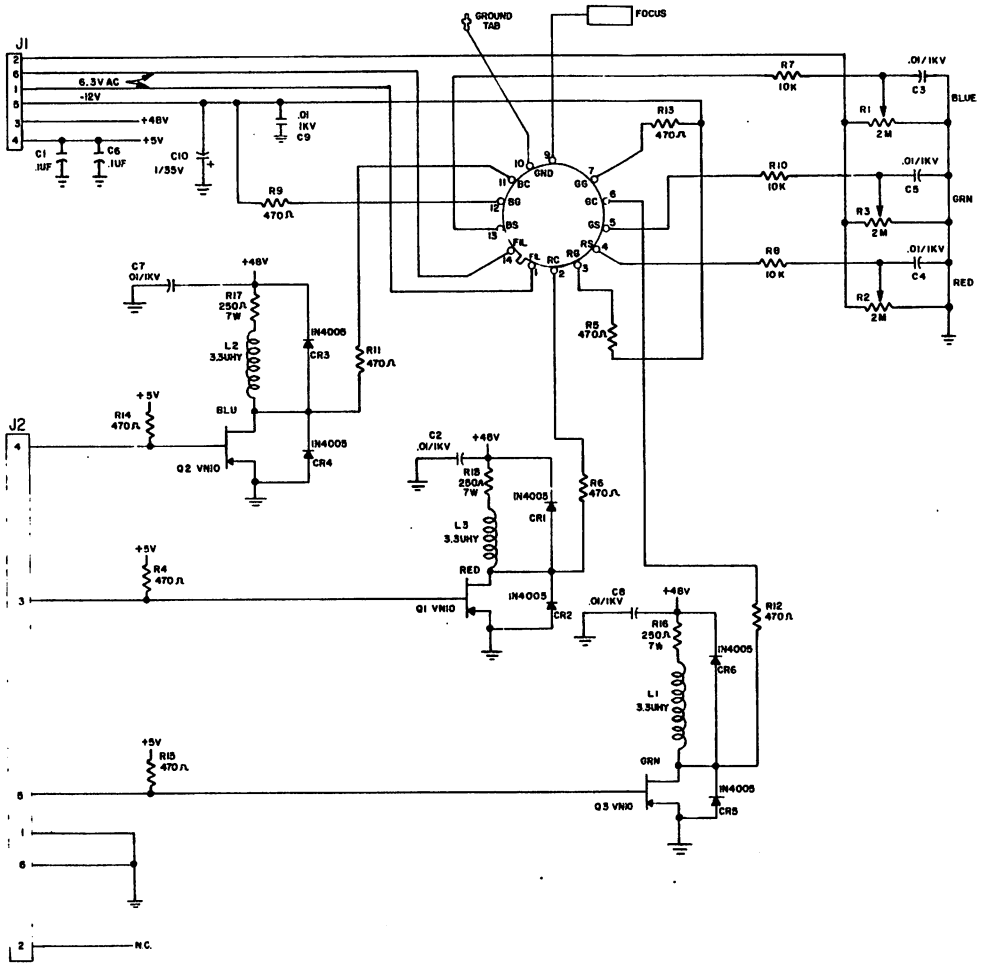
Intelligent Systems Corp.®

SCHEMATIC DYNAMIC CONVERGENCE CARD — DCCB

SIZE	CODE IDENT NO.	DRAWING NO	REV
D		101162 4	2

SCALE ~ SHEET 1 OF 1

REV		ECN		
1	ENGR. RELEASE	2097	1-1-79	
2	ADD C10	2599	2-19-82	



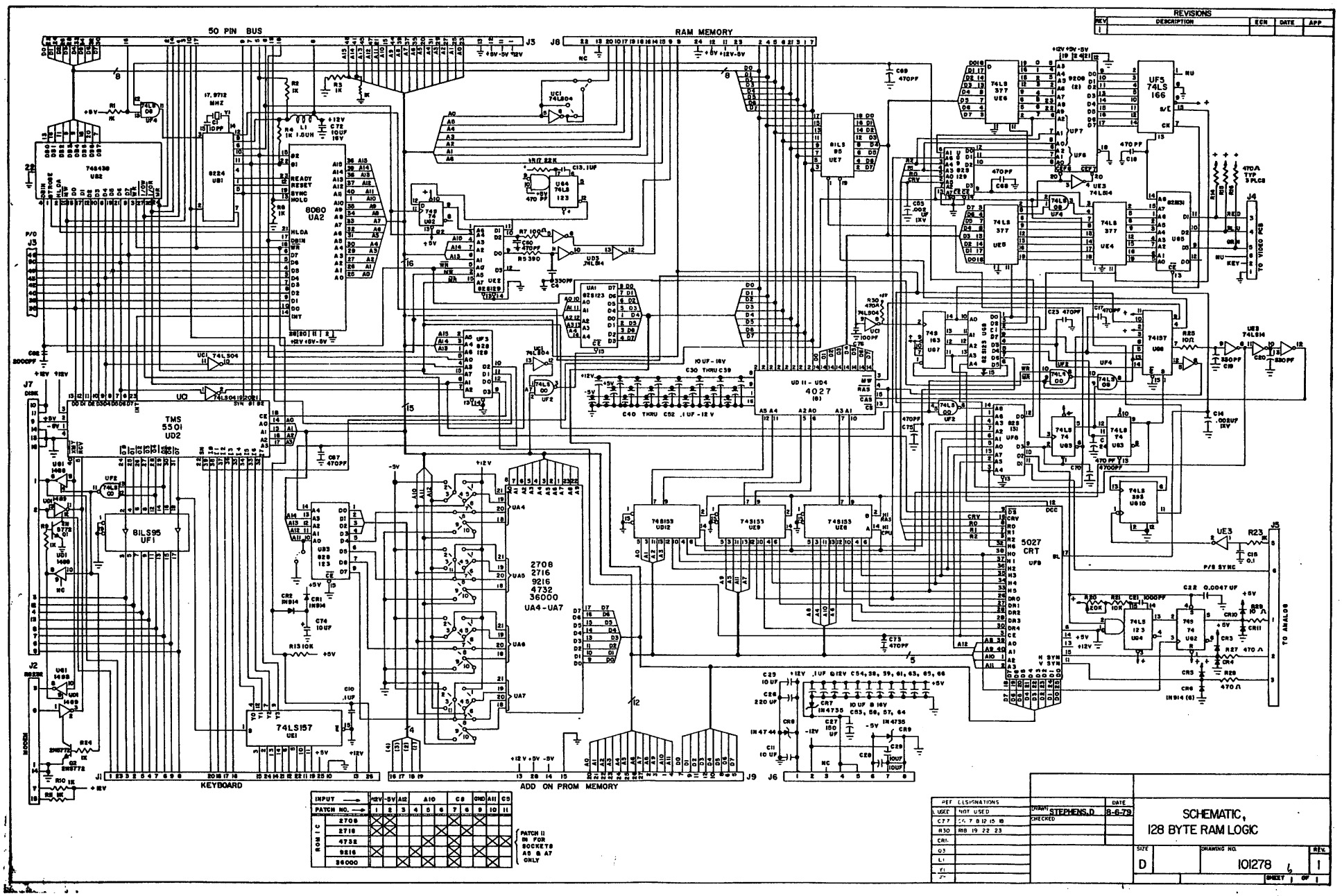
LAST USED	NOT USED
R18	
C10	
CR6	
L3	
Q3	
J2	

DRAWN	DUANE STEPHENS 10-25-79

Intelligent Systems Corp.

SCHEMATIC
VIDEO DRIVER
3000/9000

SIZE		DWG NO	REV
D		101174 5	2


50 PIN BUS
RAM MEMORY
REVISIONS
REV
DESCRIPTION
ECN
DATE
APP
8080 UA2
TMS 5501 UD2
8ILS95 UF1
74LS157 UE1
2708 2716 9216 4732 36000 UA4-UA7
UD1 - UD4 4027 (8)
5027 CRT UF8
KEYBOARD
ADD ON PROM MEMORY
TO VIDEO PCB
TO ANALOG
INPUT
PATCH NO.
ROM IC
2708
2716
4732
9216
36000
PATCH 11 IN FOR SOCKETS A9 & A7 ONLY
REF DESIGNATIONS
DRAWN STEPHENS.D
DATE 8-6-79
CHECKED
SCHEMATIC,
128 BYTE RAM LOGIC
SIZE D
DRAWING NO. 101278
REV 1
SHEET 1 OF 1

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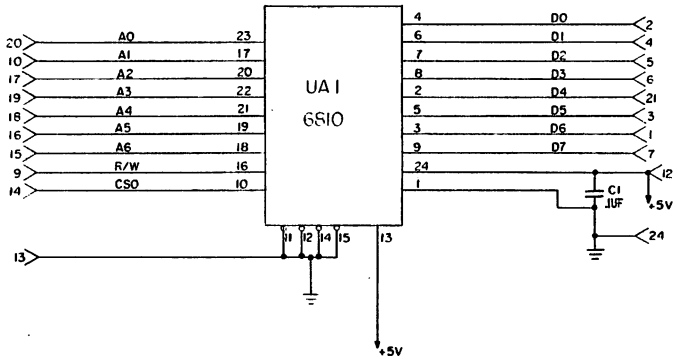
1		ENGR. RELEASE	2160	9-10-78	



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN L. Taylor	9/14/78
CHECKED	

Intelligent Systems Corp.

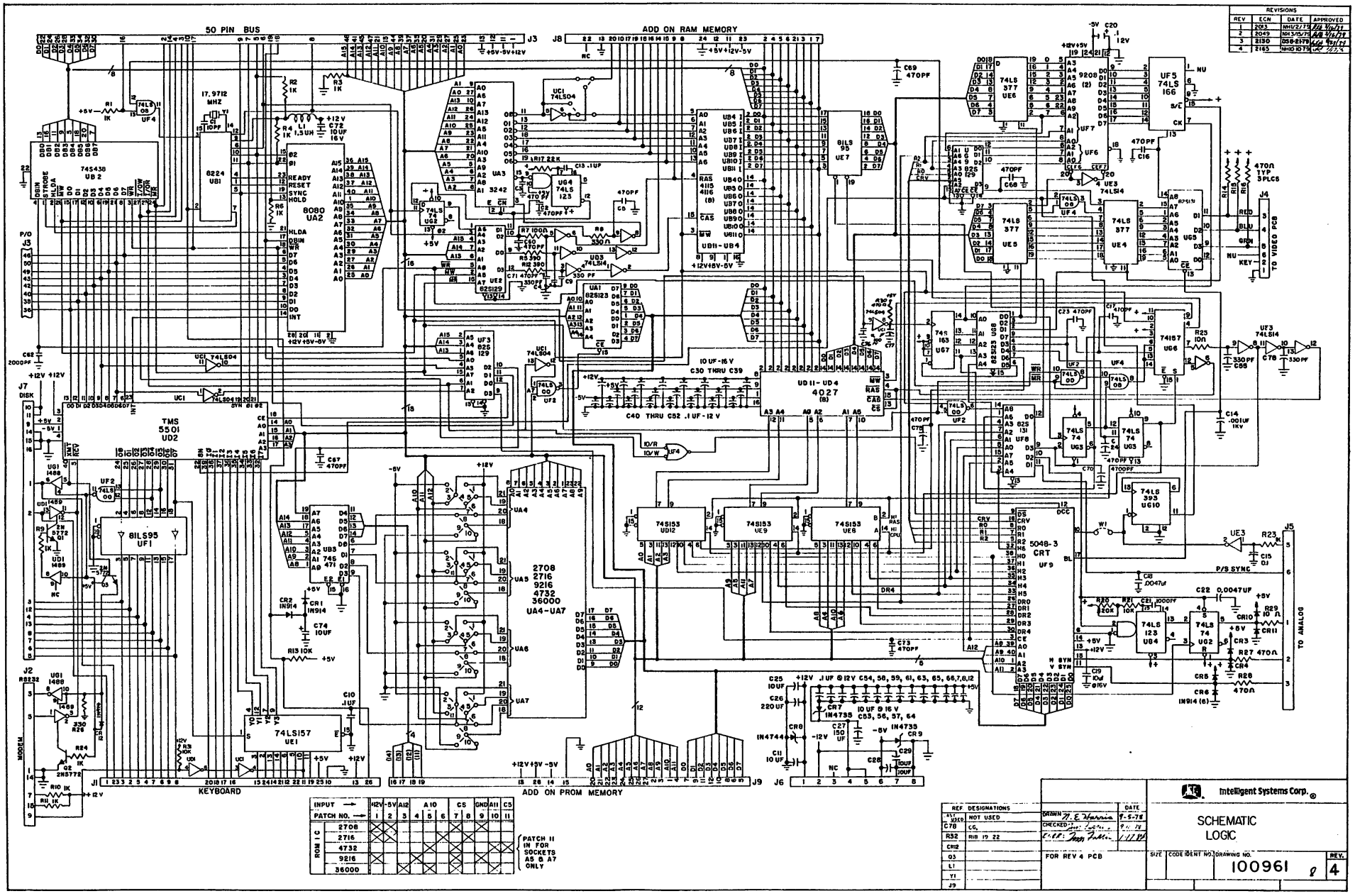
ADD ON RAM
SCHEMATIC
3000

SIZE	CODE IDENT NO	DRAWING NO.	REV
D		101043 7	1

SCALE NONE SHEET 1 OF

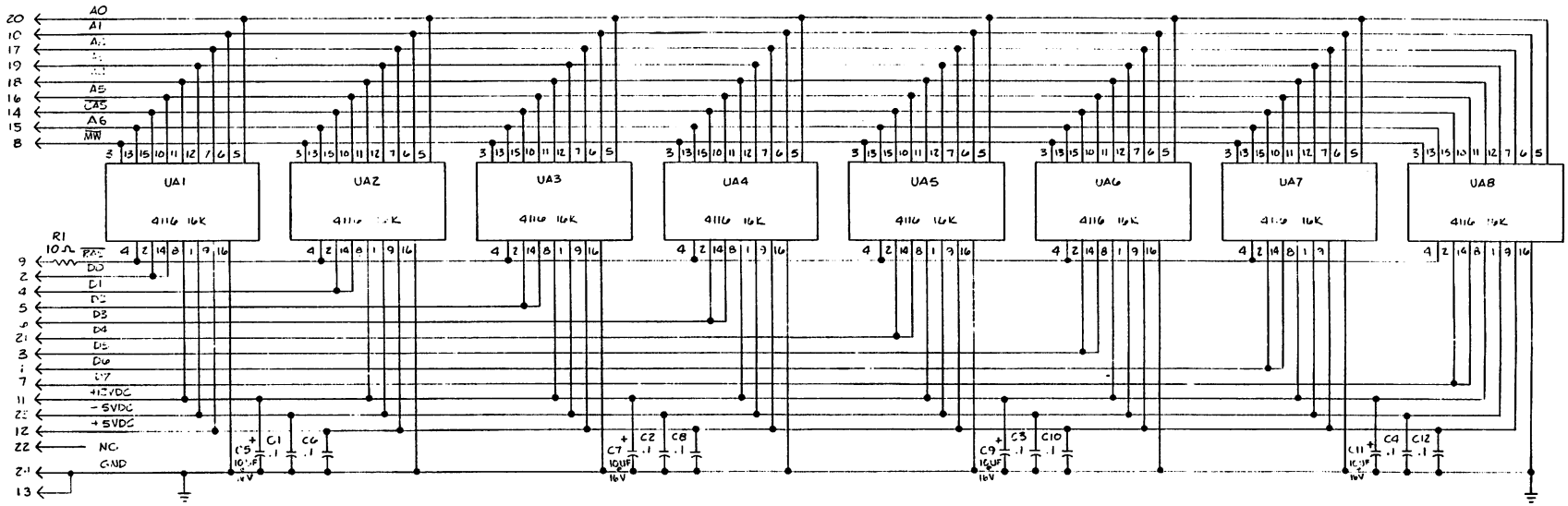
NEXT ASSY	USED ON
APPLICATION	

101043



REVISIONS			
REV	ECN	DATE	APPROVED
1	2043	NOV 12/78	
2	2049	NOV 5/79	
3	2130	DEC 21 79	
4	2165	NOV 10 79	

REV ZONE		REVISIONS DESCRIPTION	ECN	DATE	APPROVED
	1	ADD C13 CHG R1 (WAS 47Ω) CHG PIN NOS. 8, 13, 14 & 15		8-28-78	
	2	REMOVED 4K & 8K REFERENCE	2013	2-21-79	
	3	TO IOUF16V		5-23-79	



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX ±
XXX ±

CONTRACT NO

APPROVALS	DATE
DRAWN	6-16-78
CHECKED	7-13-78
ENGR	

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

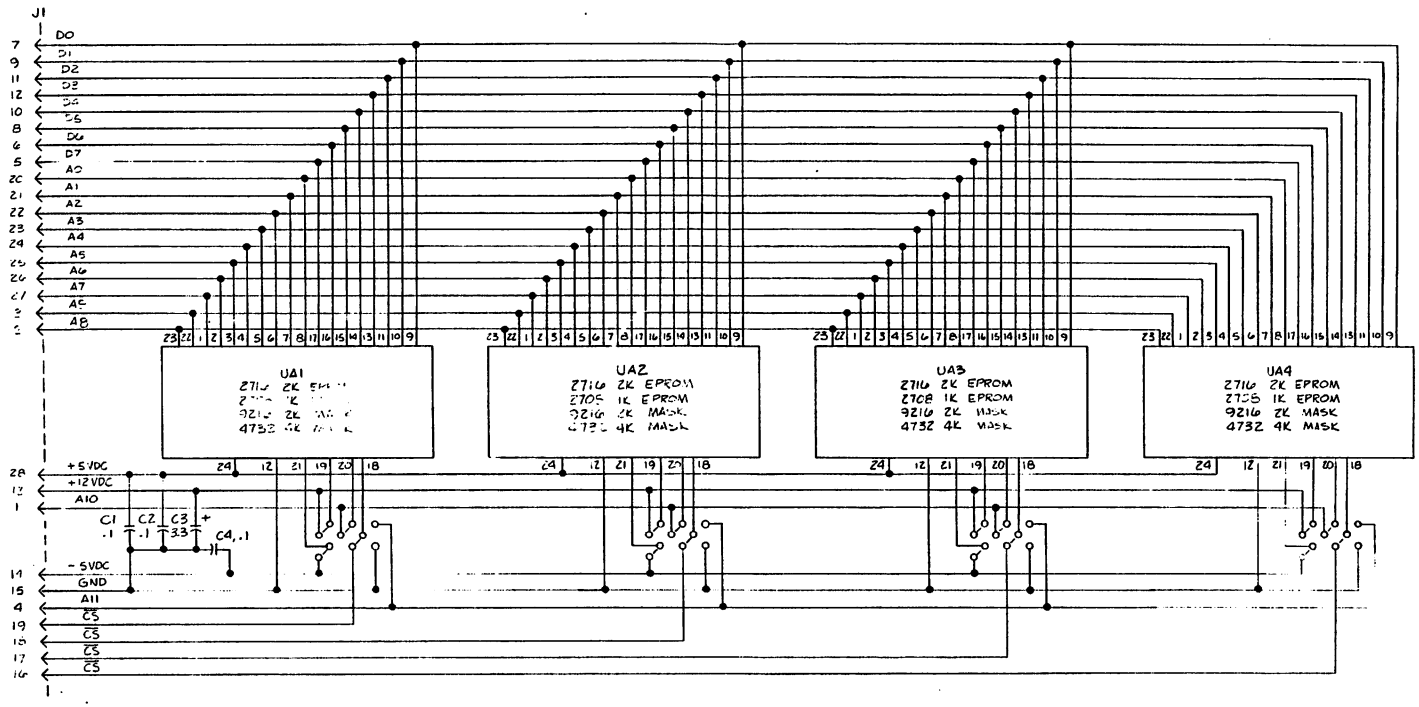
Intelligent Systems Corp.®

SCHEMATIC ADD ON RAM CONTROLLER II

SIZE	CODE IDENT NO	DRAWING NO.	REV
D		100984	3

SCALE | SHEET OF

REVISIONS					
ZONE	LTR	DESCRIPTION	ECN	DATE	APPROVED
1		ENGINEERING RELEASE	1228	3/22/82	[illegible]



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
. XX
XXX -

CONTRACT NO

APPROVALS | DATE

DRAWN

CHECKED 7-12-78

ENGR: 7-22-80

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

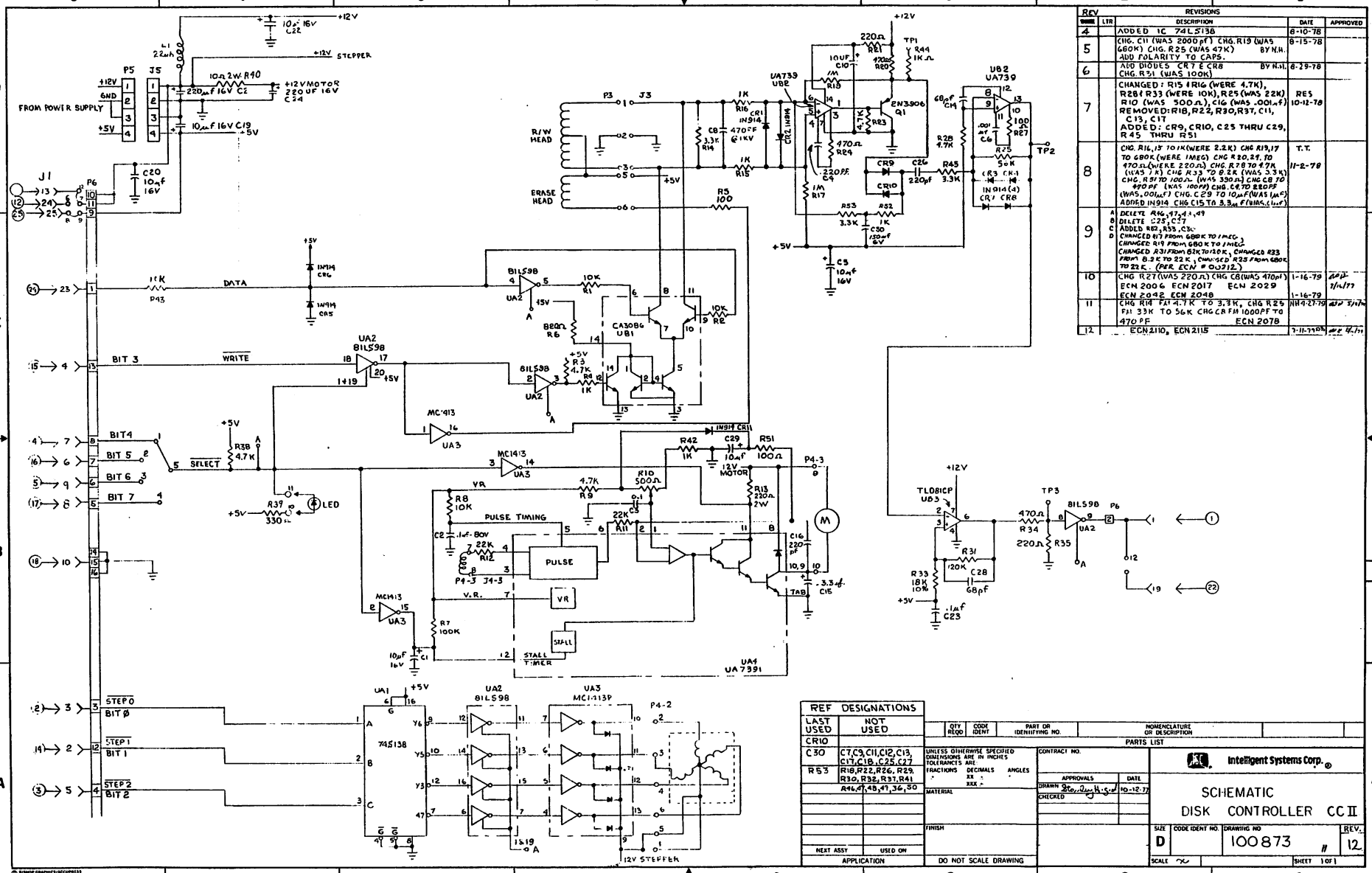
DO NOT SCALE DRAWING

Intelligent Systems Corp.®

COMPUCOLOR II ADD ON PROM SCHEMATIC DIAGRAM

SIZE	CODE IDENT NO	DRAWING NO	REV
D		100979 10	1

SCALE [illegible] SHEET 1 OF 1



REV	LTR	DESCRIPTION	DATE	APPROVED
4		ADDED IC 74LS138	8-10-78	
5		CHG. C11 (WAS 2000pF) CHG. R19 (WAS 680K) CHG. R25 (WAS 47K) BY N.H. ADD POLARITY TO CAPS.	8-15-78	
6		ADD DIODES CR7 & CR8 BY N.H. CHG. R51 (WAS 100K)	8-29-78	
7		CHANGED: R15 & R16 (WERE 4.7K), R28 & R33 (WERE 10K), R25 (WAS 22K) R10 (WAS 500Ω), C16 (WAS .001µF) REMOVED: R18, R22, R26, R29, R30, R32, R37, R41, C11, C13, C17 ADDED: CR9, CR10, C25 THRU C29, R45 THRU R51	RES 10-12-78	
8		CHG. R16, 17 TO 1K (WERE 2.2K) CHG R19, 17 TO 680K (WERE 1MEG) CHG R20, 29, TO 470Ω (WERE 220Ω) CHG R28 TO 4.7K (WAS 7K) CHG R33 TO 8.2K (WAS 3.3K) CHG. R37 TO 100Ω (WAS 330Ω) CHG C8 TO 470 PF (WAS 100PF) CHG. C4 TO 220PF (WAS .001µF) CHG. C29 TO 10µF (WAS 1µF) ADDED IN914 CHG C15 TO 3.3µF (WAS .1µF)	T.T. 11-2-78	
9	A B C D	DELETE R46, 47, 48, 49 DELETE C25, C27 ADDED R52, R53, C30 CHANGED R17 FROM 680K TO 1MEG CHANGED R19 FROM 680K TO 1MEG CHANGED R31 FROM 82K TO 120K, CHANGED R33 FROM 8.2K TO 22K, CHANGED R25 FROM 680K TO 22K. (PER ECN # 00212)		
10		CHG R27 (WAS 220Ω) CHG C8 (WAS 470pF) ECN 2006 ECN 2017 ECN 2029 ECN 2042 ECN 2048	1-16-79	
11		CHG R14 FR 4.7K TO 3.3K, CHG R25 FR 33K TO 56K CHG CR FM 1000PF TO 470 PF ECN 2078	1-16-79	
12		ECN 2110, ECN 2115	3-11-79	

REF DESIGNATIONS	
LAST USED	NOT USED
CR10	
C30	C7, C9, C11, C12, C13, C17, C18, C25, C27
R53	R18, R22, R26, R29, R30, R32, R37, R41 R46, 47, 48, 49, 36, 50

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

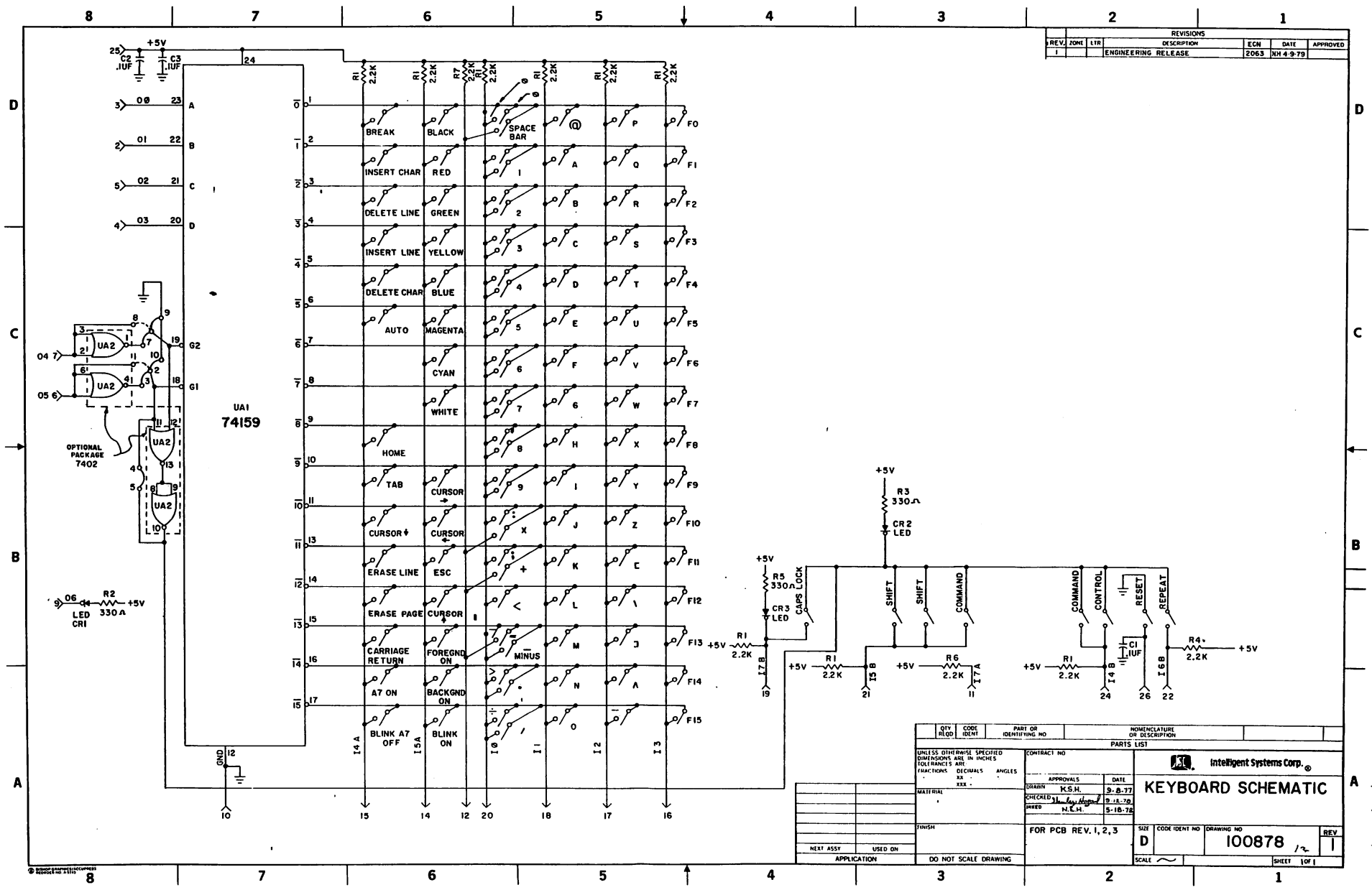
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
. XX .
XXX .
MATERIAL
FINISH
NEXT ASSY USED ON
APPLICATION
DO NOT SCALE DRAWING

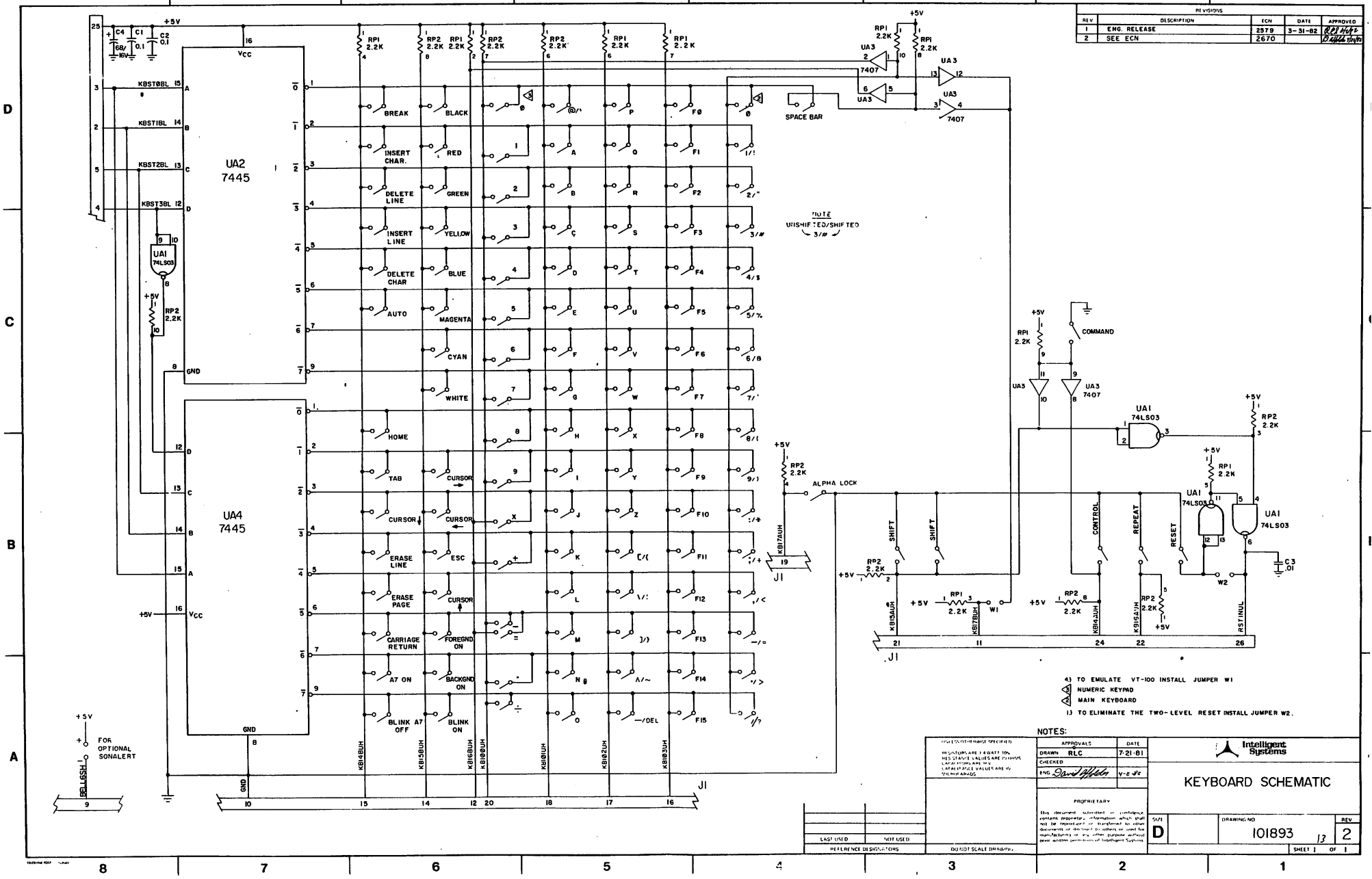
CONTRACT NO.
APPROVALS DATE
DRAWN 10-12-77
CHECKED

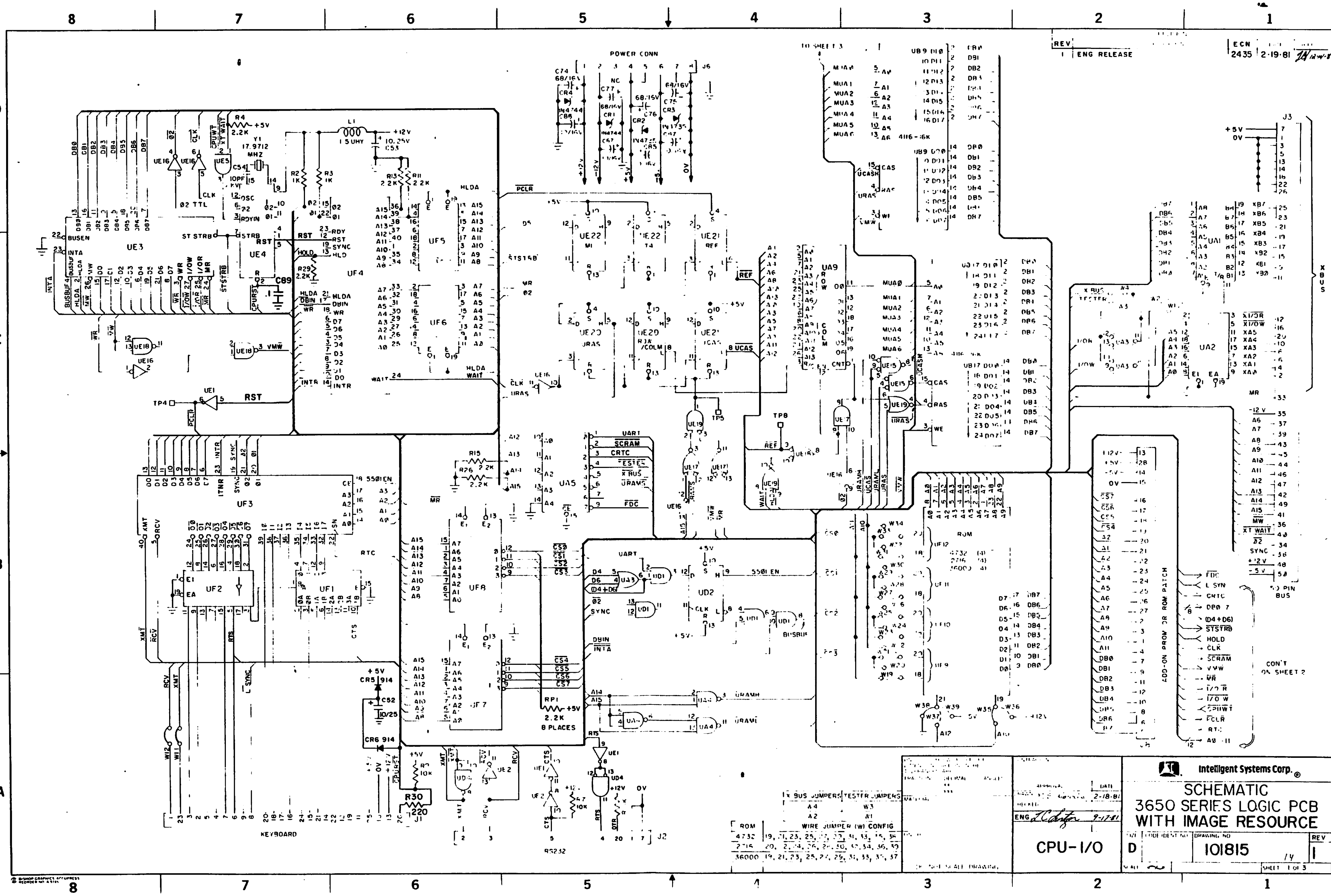
Intelligent Systems Corp.

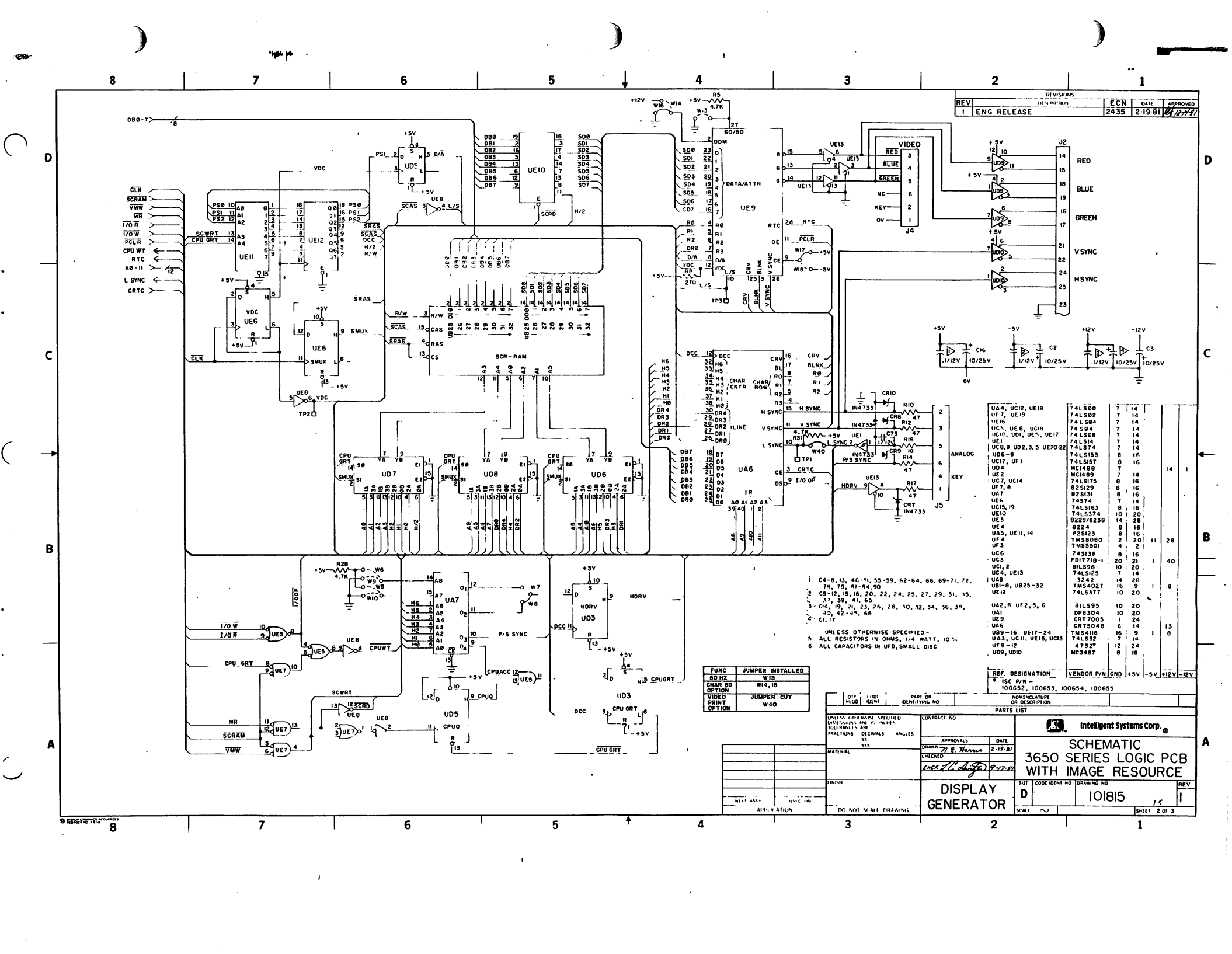
SCHEMATIC
DISK CONTROLLER CC II

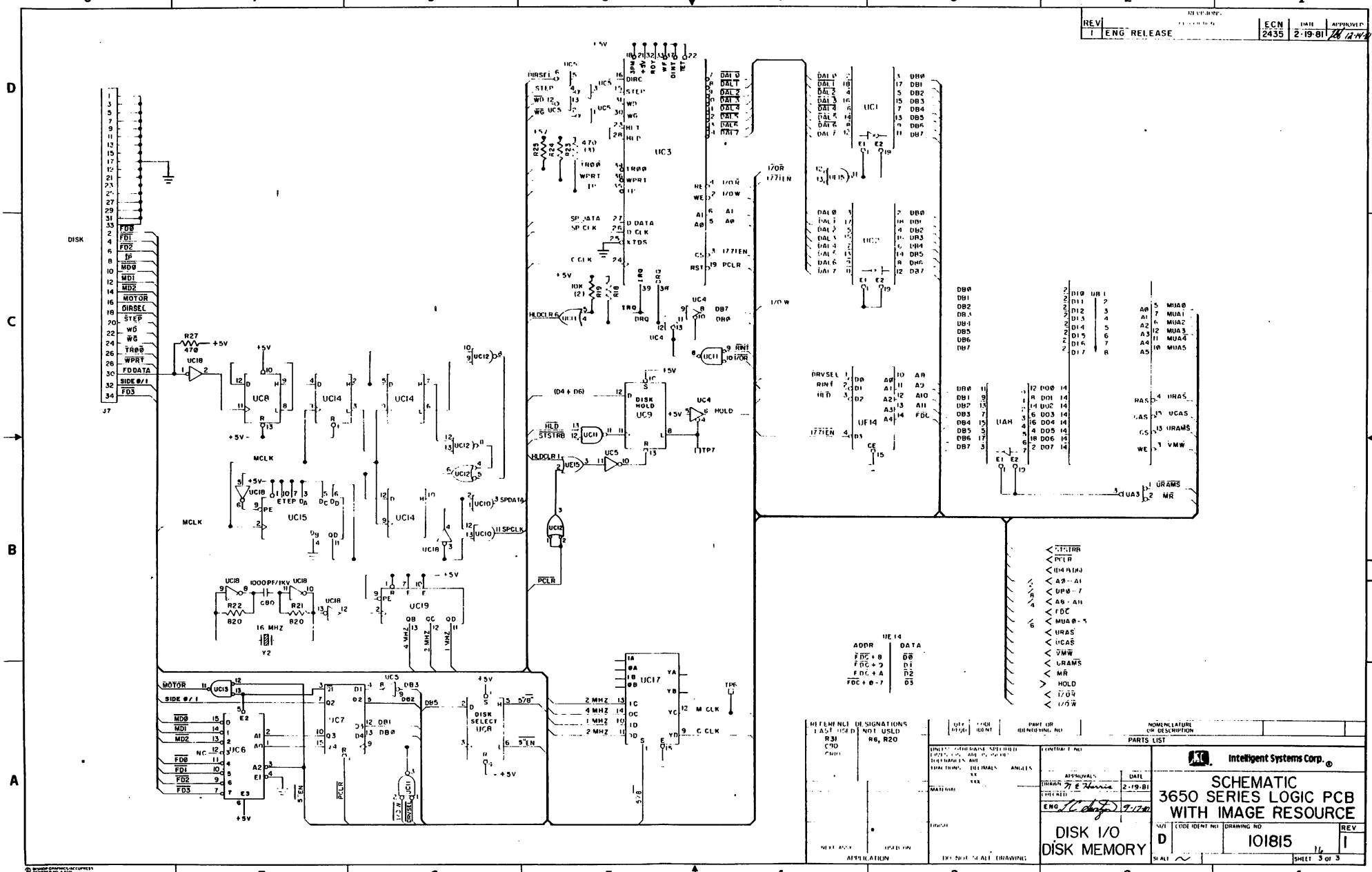
SIZE D | CODE IDENT NO. | DRAWING NO 100873 | REV. 12
SCALE | SHEET 1 OF 1

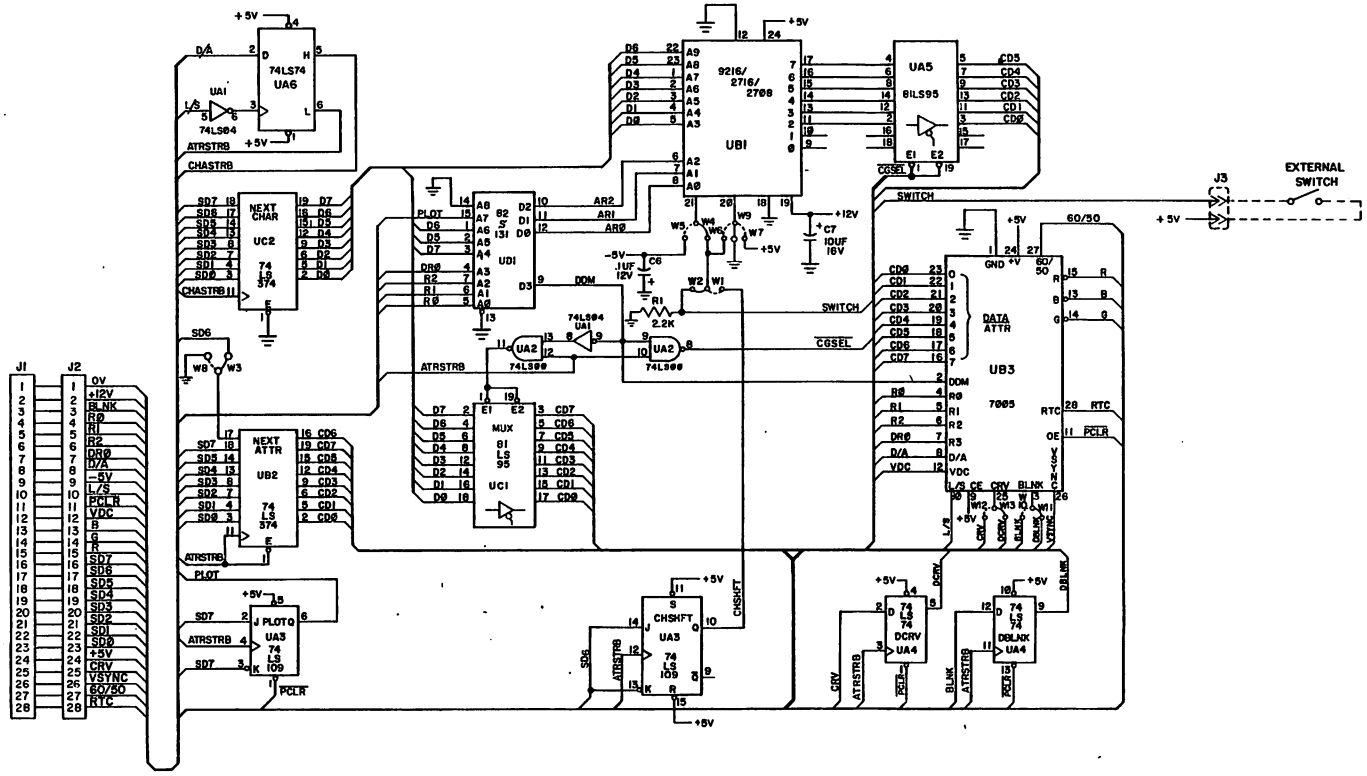

REVISIONS
REV. ZONE LTR DESCRIPTION ECN DATE APPROVED
1 ENGINEERING RELEASE 2063 NH 4-9-79
+5V
C2 .1UF
C3 .1UF
UA1 74159
OPTIONAL PACKAGE 7402
UA2
R1 2.2K
R7 2.2K
BREAK
INSERT CHAR
DELETE LINE
INSERT LINE
DELETE CHAR
AUTO
HOME
TAB
CURSOR→
CURSOR↑
CURSOR←
ESC
ERASE LINE
ERASE PAGE
CURSOR↓
CARRIAGE RETURN
A7 ON
BLINK A7 OFF
BLACK
RED
GREEN
YELLOW
BLUE
MAGENTA
CYAN
WHITE
BACKGND ON
BLINK ON
FOREGND ON
SPACE BAR
MINUS
LED CR1
R2 330Ω
R3 330Ω
CR2 LED
R5 330Ω
CAPS LOCK
CR3 LED
SHIFT
SHIFT
COMMAND
COMMAND
CONTROL
RESET
REPEAT
R6 2.2K
R4 2.2K
C1 .1UF
GND
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.01 .XXX ±.005
MATERIAL
FINISH
NEXT ASSY USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS DATE
DRAWN K.S.H. 9-8-77
CHECKED 9-12-78
ISSUED N.E.H. 5-18-78
FOR PCB REV. 1, 2, 3
Intelligent Systems Corp.
KEYBOARD SCHEMATIC
SIZE D
CODE IDENT NO
DRAWING NO 100878 /2
REV 1
SCALE
SHEET 1 OF 1


REVISIONS
REV | DESCRIPTION | ECN | DATE | APPROVED
1 | ENG. RELEASE | 2579 | 3-31-82 | RLC Hight D Allen Hyde
2 | SEE ECN | 2670 | |
UA2 7445
UA4 7445
UA1 74LS03
UA3 7407
BREAK
BLACK
INSERT CHAR.
RED
DELETE LINE
GREEN
INSERT LINE
YELLOW
DELETE CHAR
BLUE
AUTO
MAGENTA
CYAN
WHITE
HOME
TAB
CURSOR
CURSOR
CURSOR
ESC
ERASE LINE
ERASE PAGE
CURSOR
CARRIAGE RETURN
FOREGND ON
A7 ON
BACKGND ON
BLINK A7 OFF
BLINK ON
SPACE BAR
ALPHA LOCK
SHIFT
SHIFT
CONTROL
REPEAT
RESET
COMMAND
NOTE
UNSHIFTED/SHIFTED
FOR OPTIONAL SONALERT
4) TO EMULATE VT-100 INSTALL JUMPER W1
NUMERIC KEYPAD
MAIN KEYBOARD
13) TO ELIMINATE THE TWO-LEVEL RESET INSTALL JUMPER W2.
NOTES:
APPROVALS | DATE
DRAWN RLC | 7-21-81
CHECKED
ENG David Hyde | 4-6-82
PROPRIETARY
Intelligent Systems
KEYBOARD SCHEMATIC
SIZE D
DRAWING NO 101893 13
REV 2
SHEET 1 OF 1


Intelligent Systems Corp.
SCHEMATIC
3650 SERIES LOGIC PCB
WITH IMAGE RESOURCE
CPU-I/O
D
101815
REV 1
SHEET 1 OF 3
REV 1 ENG RELEASE
ECN 2435 2-19-81
POWER CONN
KEYBOARD
RS232
ADD-ON PROM OR ROM PATCH
CON'T ON SHEET 2
50 PIN BUS
X BUS


REVISIONS
REV | DESCRIPTION | ECN | DATE | APPROVED
1 | ENG RELEASE | 2435 | 2-19-81
SCHEMATIC
3650 SERIES LOGIC PCB
WITH IMAGE RESOURCE
DISPLAY
GENERATOR
Intelligent Systems Corp.
SIZE D | DRAWING NO 101815 | REV 1
SHEET 2 OF 3
DRAWN T. E. Harris 2-19-81
CHECKED
ENGR
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS | DATE
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
PARTS LIST
QTY REQD | ITEM IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX
XXX
DB0-7
CLK
SCRAM
VMW
MR
I/O R
I/O W
PCLR
CPU WT
RTC
A0-11
L SYNC
CRTC
VDC
SCWRT
CPU GRT
SRAS
SCAS
R/W
SCR-RAM
CHAR CNTR
CHAR ROW
H SYNC
V SYNC
L SYNC
P/S SYNC
HDRV
CPUACC
CPUWT
CPUGRT
VIDEO
RED
BLUE
GREEN
NC
KEY
OV
VSYNC
HSYNC
ANALOG KEY
+5V
-5V
+12V
-12V
W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 W12 W13 W14 W15 W16 W17 W18
W40
R5 4.7K
R10 R11 R12 R13 R14 R15 R16 R17 R31 R28
C16 .1/12V 10/25V
C2 1/12V 10/25V
C3 1/12V 10/25V
C73 1/12V
CR7 CR8 CR9 CR10 IN4733
TP1 TP2 TP3
J2 J4 J5
UE1 UE6 UE8 UE9 UE10 UE11 UE12 UE13
UD3 UD5 UD7 UD8 UD6
UA6 UA7
UD1 UD2 UD4 UD9 UD10
1 C4-8, 13, 46-51, 55-59, 62-64, 66, 69-71, 72, 74, 79, 81-84, 90
2 C9-12, 15, 16, 20, 22, 24, 25, 27, 29, 31, 35, 37, 39, 41, 65
3 C14, 19, 21, 23, 26, 28, 30, 32, 34, 36, 38, 40, 42-45, 68
4 C1, 17
5 UNLESS OTHERWISE SPECIFIED - ALL RESISTORS IN OHMS, 1/4 WATT, 10%
6 ALL CAPACITORS IN UFD, SMALL DISC
FUNC | JUMPER INSTALLED
60 HZ | W15
CHAR BD OPTION | W14, 18
VIDEO PRINT OPTION | JUMPER CUT W40
REF. DESIGNATION | VENDOR P/N | GND | +5V | -5V | +12V | -12V
* ISC P/N - 100652, 100653, 100654, 100655
UA4, UC12, UE18 | 74LS00 | 7 | 14
UF7, UE19 | 74LS02 | 7 | 14
UE16 | 74LS04 | 7 | 14
UC5, UE8, UC18 | 74S04 | 7 | 14
UC10, UD1, UE5, UE17 | 74LS08 | 7 | 14
UE1 | 74LS14 | 7 | 14
UC8,9 UD2,3,5 UE20 22 | 74LS74 | 7 | 14
UD6-8 | 74LS153 | 8 | 16
UC17, UF1 | 74LS157 | 8 | 16
UD4 | MC1488 | 7 | 14
UE2 | MC1489 | 7 | 14
UC7, UC14 | 74LS175 | 8 | 16
UF7, 8 | 82S129 | 8 | 16
UA7 | 82S131 | 8 | 16
UE6 | 74S74 | 7 | 14
UC15, 19 | 74LS163 | 8 | 16
UE10 | 74LS374 | 10 | 20
UE3 | 8229/8238 | 14 | 28
UE4 | 8224 | 8 | 16
UA5, UE11, 14 | 82S123 | 8 | 16
UF4 | TMS8080 | 2 | 20 | 11 | 28
UF3 | TMS5501 | 4 | 2 | 1
UC6 | 74S138 | 8 | 16
UC3 | FD1771B-1 | 20 | 21 | 1 | 40
UC1, 2 | 81LS98 | 10 | 20
UC4, UE13 | 74LS125 | 7 | 14
UA9 | 3242 | 14 | 28
UB1-8, U825-32 | TMS4027 | 16 | 9 | 1 | 8
UE12 | 74LS377 | 10 | 20
UA2,8 UF2,5,6 | 81LS95 | 10 | 20
UA1 | DP8304 | 10 | 20
UE9 | CRT7005 | 1 | 24
UA6 | CRT5048 | 6 | 14 | 13
UB9-16 UB17-24 | TMS4116 | 16 | 9 | 1 | 8
UA3, UC11, UE15, UC13 | 74LS32 | 7 | 14
UF9-12 | 4732* | 12 | 24
UD9, UD10 | MC3487 | 8 | 16


REV
ECN
DATE
APPROVED
1 ENG RELEASE
2435
2-19-81
DISK
J7
UC1
UC2
UC3
UC4
UC5
UC6
UC7
UC8
UC9
UC10
UC11
UC12
UC13
UC14
UC15
UC16
UC17
UC18
UC19
UE14
UF14
UAH
UA3
Y2
16 MHZ
R22
820
R21
820
C80
1000PF/1KV
R27
470
MCLK
PCLR
HOLD
I/OR
I/OW
1771EN
M CLK
C CLK
SCHEMATIC
3650 SERIES LOGIC PCB
WITH IMAGE RESOURCE
DISK I/O
DISK MEMORY
101815
SHEET 3 OF 3
Intelligent Systems Corp.



TABLE

DEVICE	JUMPER
UB1 9216	W4, W9
UB1 2716	W5, W6
UB1 2708	W5, W9
UB1 9216P	W4, W7

DEVICE	JUMPER
HARDWARE SWITCH	W2, W3
SOFTWARE SWITCH	W1, W8

REVISIONS						
REV	ZONE	LTR	DESCRIPTION	ECN	DATE	APPROVED
1			ENG. RELEASE	2415	1-6-81	
2			CORRECT JUMPER TRACES	2430	11-23-81	

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
. XX .
. XXX .

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN TAYLOR	1/7/80
CHECKED ENGR. K.C. Schultz	1-6-81

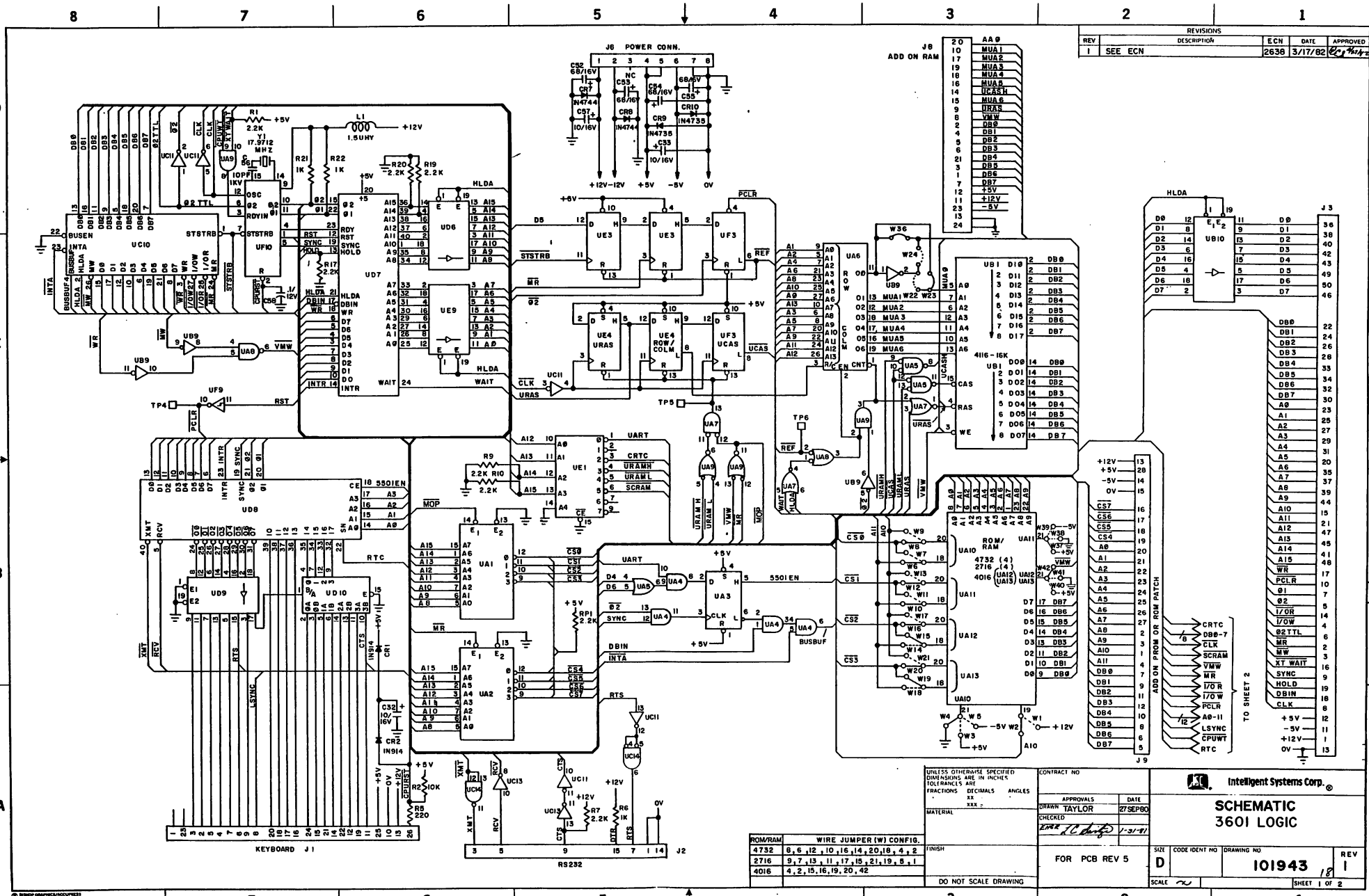
FOR REV 1 & 2 PCB

Intelligent Systems Corp.

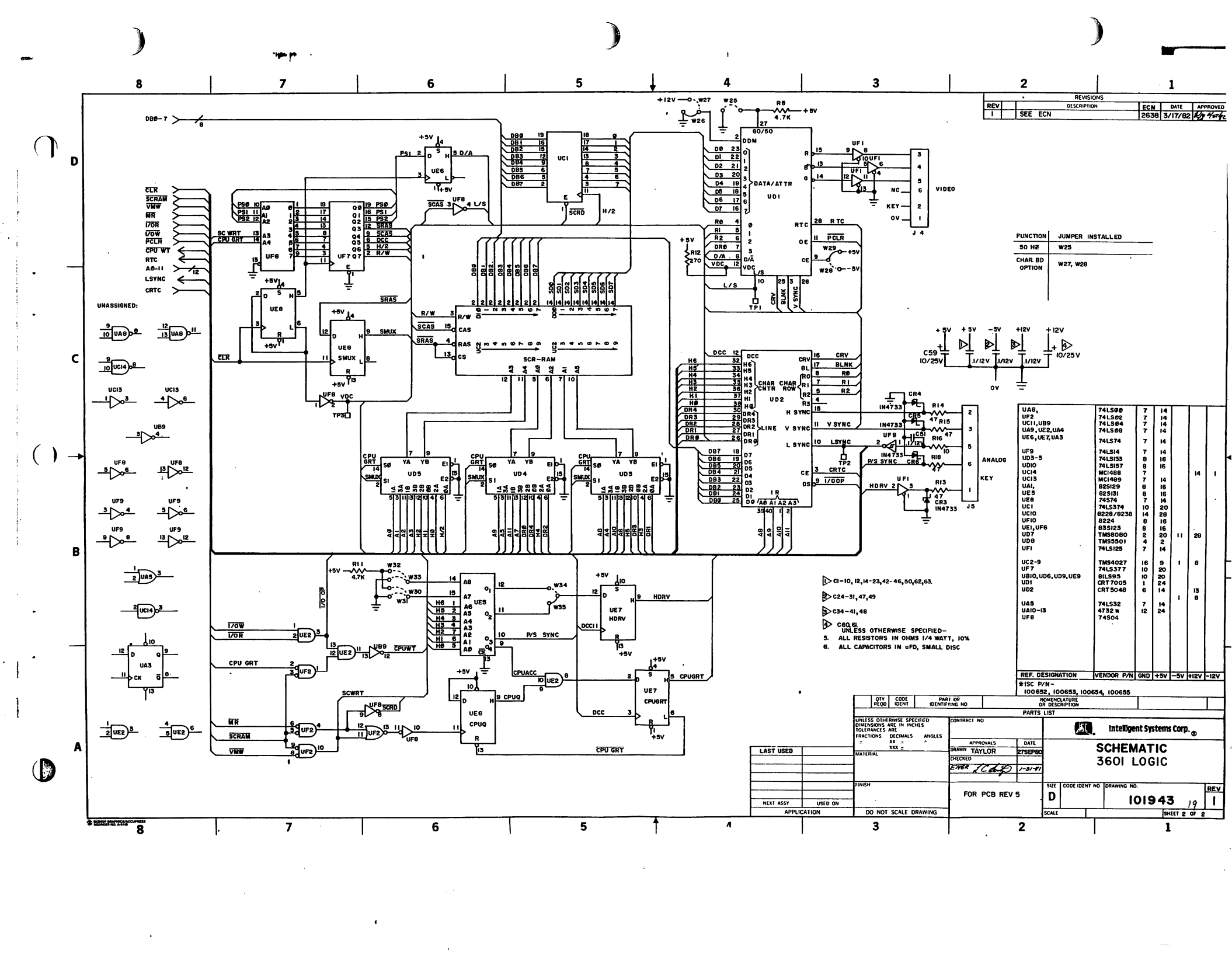
SCHEMATIC
OPTIONAL CHARACTER GENERATOR

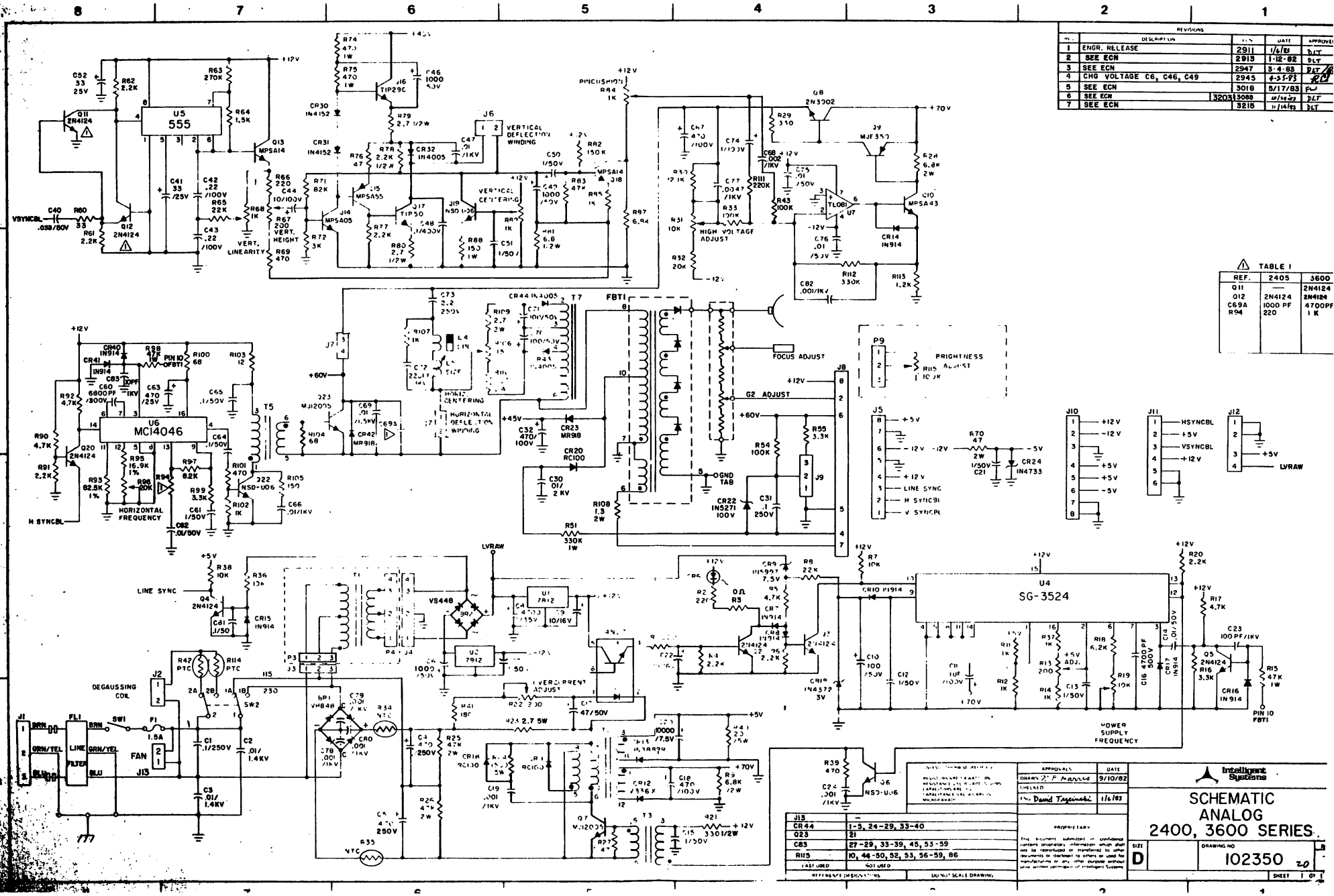
SIZE	CODE IDENT NO	DRAWING NO.	REV
D		101410 17	2

SCALE NONE | SHEET 1 OF 1

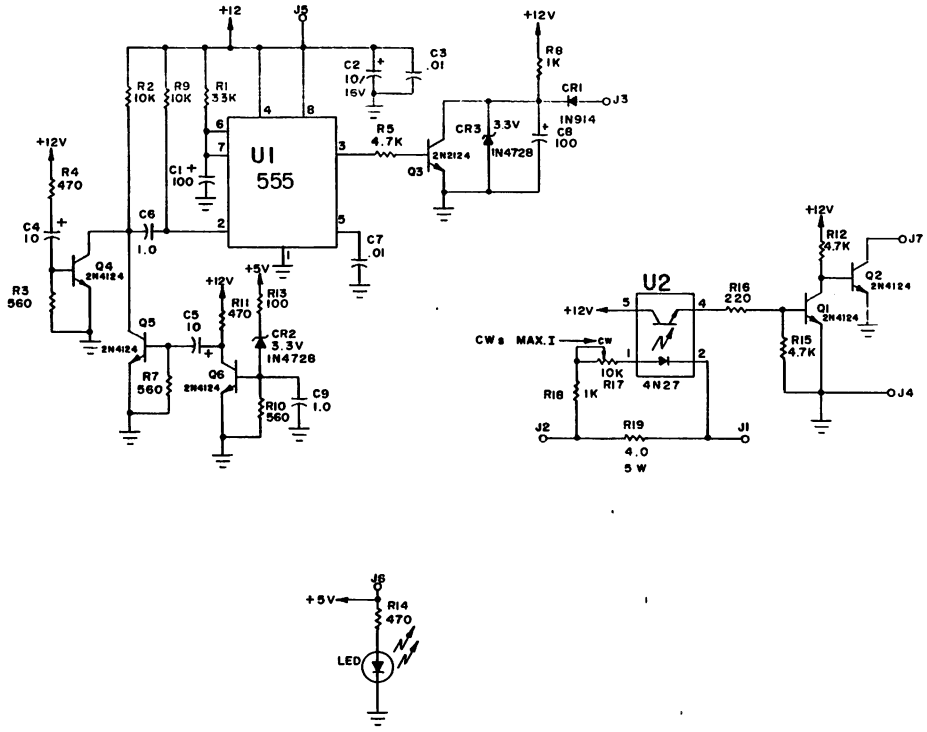


REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	SEE ECN	2638	3/17/82	


REVISIONS
REV | DESCRIPTION | ECN | DATE | APPROVED
1 | SEE ECN | 2638 | 3/17/82
FUNCTION | JUMPER INSTALLED
50 HZ | W25
CHAR. BD OPTION | W27, W28
SCHEMATIC
3601 LOGIC
Intelligent Systems Corp.
FOR PCB REV 5
101943
SHEET 2 OF 2
PARTS LIST
REF. DESIGNATION | VENDOR P/N | GND | +5V | -5V | +12V | -12V
*ISC P/N-
100652, 100653, 100654, 100655
5. ALL RESISTORS IN OHMS 1/4 WATT, 10%
6. ALL CAPACITORS IN uFD, SMALL DISC
UNASSIGNED:
SCR-RAM
CHAR CNTR
CHAR ROW
LINE CNTR
DATA/ATTR
VIDEO
ANALOG KEY
UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DRAWING


REVISIONS
NO. DESCRIPTION ECN DATE APPROVED
1 ENGR. RELEASE 2911 1/6/82 PLT
2 SEE ECN 2913 1-12-82 PLT
3 SEE ECN 2947 3-4-83 PLT
4 CHG VOLTAGE C6, C46, C49 2945 4-25-83 PLT
5 SEE ECN 3018 5/17/83 PLT
6 SEE ECN 3203 3088 10/24/83 PLT
7 SEE ECN 3215 11/14/83 PLT
TABLE I
REF. 2405 3600
Q11 — 2N4124
Q12 2N4124 2N4124
C69A 1000 PF 4700PF
R94 220 1 K
U5 555
U6 MC14046
U4 SG-3524
U1 7812
U2 7912
VERTICAL DEFLECTION WINDING
VERTICAL CENTERING
VERT. LINEARITY
VERT. HEIGHT
HIGH VOLTAGE ADJUST
FOCUS ADJUST
G2 ADJUST
BRIGHTNESS ADJUST
HORIZONTAL FREQUENCY
HORIZONTAL CENTERING
HORIZONTAL DEFLECTION WINDING
DEGAUSSING COIL
VERT. CURRENT ADJUST
POWER SUPPLY FREQUENCY
+5V ADJ.
LINE SYNC
VSYNCBL
HSYNCBL
LVRAW
PIN 10 FBT1
FAN
J13
J1 J2 J3 J4 J5 J6 J7 J8 J9 J10 J11 J12
T1 T2 T3 T4 T5 T6 T7
FBT1
Intelligent Systems
SCHEMATIC
ANALOG
2400, 3600 SERIES
SIZE D
DRAWING NO 102350 20
SHEET 1 OF 1
APPROVALS DATE
DRAWN 9/10/82
CHECKED
ENG David Tagawa 1/6/83
PROPRIETARY
J13 —
CR44 1-5, 24-29, 33-40
Q23 21
C83 27-29, 33-39, 45, 53-59
R115 10, 44-50, 52, 53, 56-59, 86
LAST USED NOT USED
REFERENCE DESIGNATIONS DO NOT SCALE DRAWING

REVISIONS				
REV	DESCRIPTION	ECN	APPROVED	DATE
1	ENG RELEASE	3633	[illegible]	11/20/84



⚠ UNLESS OTHERWISE SPECIFIED: RESISTORS ARE 1/4 WATT 5%
RESISTANCE VALUES ARE IN OHMS. CAPACITORS ARE 50V
CAPACITANCE VALUES ARE IN MICROFARADS.

	APPROVALS	DATE
DRAWN	GHB	10-2-84
CHECKED		
[illegible]	F. Winn	11/20/84

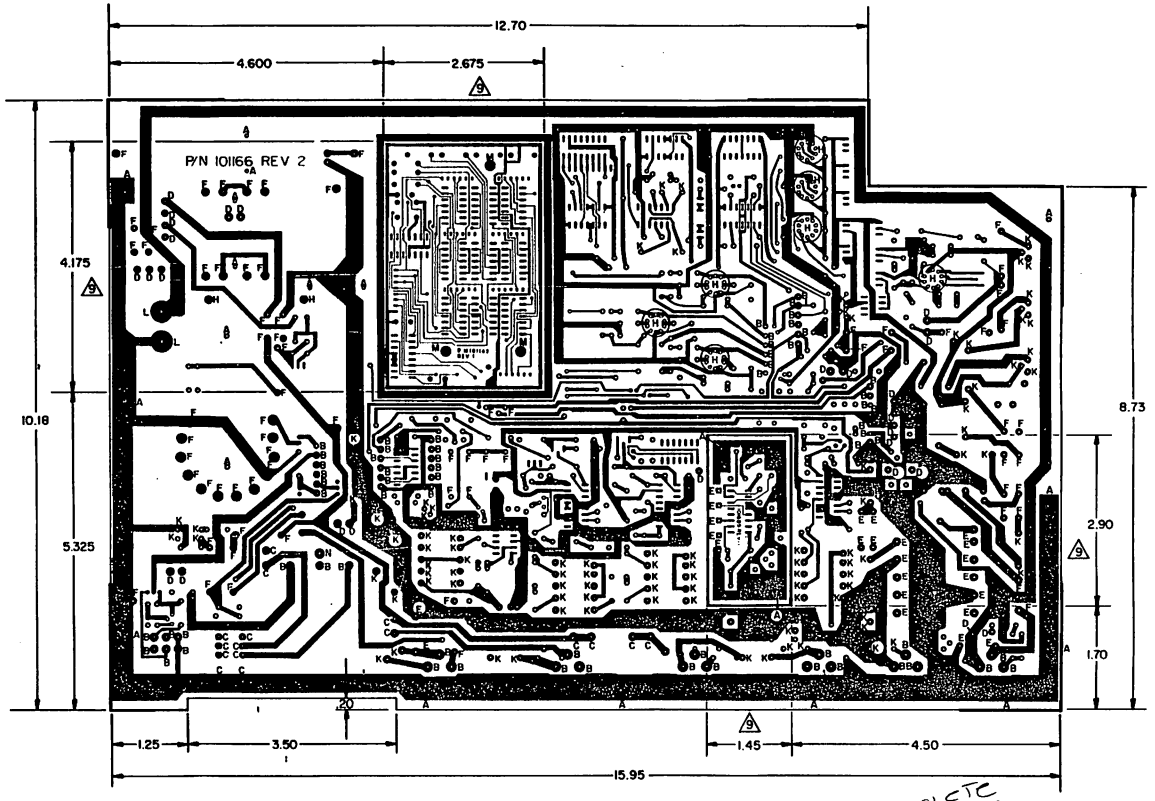
DO NOT SCALE DRAWING

Intelligent Systems

PCB SCHEMATIC
AUTO-RESTART

SIZE	DRAWING NO	REV
C	103387	1
SCALE		SHEET 1 OF 1

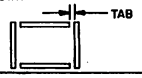
REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
2	SEE ECN	2406	12/10/80	



OBSOLETE
Per ECN 2947
DEB 3-3-83

NOTES:

1. ALL HOLES LOCATED ON .050 GRID WITHIN .005 OF THEIR TRUE POSITION UNLESS OTHERWISE SPECIFIED.
2. ALL HOLES SHALL BE PLATED THRU WITH A MINIMUM OF .001 INCH THICK COPPER.
3. FINISHED HOLE SIZE SHALL BE ± .003 OF NORMAL HOLE SIZE AFTER PLATING, WITH A MINIMUM ANNULAR RING OF .010.
4. CONNECTOR CONTACTS SHALL BE PLATED WITH GOLD OVER LOW STRESS NICKEL. GOLD PLATING SHALL BE A MINIMUM OF .00005 INCH THICK AND SHALL BE IN ACCORDANCE WITH MIL-G-45204. LOW STRESS NICKEL PLATING. SHALL BE A MINIMUM OF .0005 INCH THICK.
5. FINISH SHALL BE COPPER (EXCEPT CONNECTOR CONTACTS) PLATED WITH ELECTRODEPOSITED TIN-LEAD. PLATING SHALL BE A MINIMUM OF .0003 INCH THICK AND SHALL BE 60% ± 10% TIN.
6. MATERIAL SHALL BE FR-4 IN ACCORDANCE WITH MIL-P-13949.
7. SILKSCREEN NOMENCLATURE ON COMPONENT SIDE WITH NONCONDUCTIVE WHITE INK.
8. SOLDER MASK SHALL BE PROVIDED ON CIRCUIT SIDE (BACK) USING COLONIAL INK ER 7040 GREEN SOLDER MASK OR EQUIVALENT. LEAVE ALL PADS UNMASKED.
9. THIS AREA TO BE CUT OUT WITH UP TO 1/8" ROUTER LEAVING A TAB IN EACH CORNER OF APPROXIMATELY 1/32" AS SHOWN



SYMBOL	DESCRIPTION	QTY
UNMARKED	.032-.037	984
A	.139-.145	19
B	.072-.077	65
C	.069-.074	16
D	.063-.067	26
E	.058-.063	24
F	.051-.056	71
H	.040-.045	72
K	.037-.042	95
L	.200	2
M	.188 X .188 SQ HOLE	3
N	.100	1

NEXT ASSY | USED ON
APPLICATION

QTY REQD | ITEM IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION
PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .015 ± .XXX ± .005

MATERIAL

FINISH

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN TAYLOR	10-24-80
CHECKED	

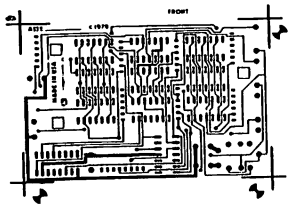
Intelligent Systems Corp.

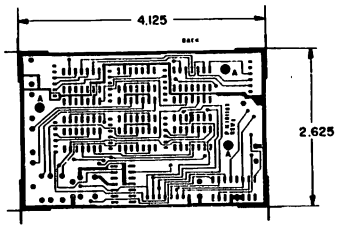
DRILL DRAWING
ANALOG MODULE

SIZE	CODE IDENT NO	DRAWING NO	REV
D		101166	2

SCALE / SHEET 1 OF 1

REVISIONS					
REV	LTR	DESCRIPTION	ECN	DATE	APPROVED
1		ENG. RELEASE	2097	5-22-79	





NOTES:

1. ALL HOLES LOCATED ON .050 GRID WITHIN .005 OF THEIR TRUE POSITION UNLESS OTHERWISE SPECIFIED.
2. ALL HOLES SHALL BE PLATED THRU WITH A MINIMUM OF .001 INCH THICK COPPER.
3. FINISHED HOLE SIZE SHALL BE ± .003 OF NORMAL HOLE SIZE AFTER PLATING, WITH A MINIMUM ANNULAR RING OF .010.
4. CONNECTOR CONTACTS SHALL BE PLATED WITH GOLD OVER LOW STRESS NICKEL. GOLD PLATING SHALL BE A MINIMUM OF .00005 INCH THICK AND SHALL BE IN ACCORDANCE WITH MIL-G-45204. LOW STRESS NICKEL PLATING. SHALL BE A MINIMUM OF .0005 INCH THICK.
5. FINISH SHALL BE COPPER (EXCEPT CONNECTOR CONTACTS) PLATED WITH ELECTRODEPOSITED TIN-LEAD. PLATING SHALL BE A MINIMUM OF .0003 INCH THICK AND SHALL BE 60% ± 10% TIN.
6. MATERIAL SHALL BE FR-4 IN ACCORDANCE WITH MIL-P-13949.
7. SILKSCREEN NOMENCLATURE ON COMPONENT SIDE WITH NONCONDUCTIVE WHITE INK.
8. SOLDER MASK SHALL BE PROVIDED ON CIRCUIT SIDE(BACK) USING COLONIAL INK ER 7040 GREEN SOLDER MASK OR EQUIVALENT. LEAVE ALL PADS UNMASKED.

PARTS LIST

SYMBOL	DESCRIPTION	QTY
UNMARKED	.032 -.036 DIA.	252
A	.188 X 188 SC.	3

T TAYLOR 1/29/79

Intelligent Systems Corp.

DRILL DRAWING CONVERGENCE PCB

SIZE	DRAWING NO	REV
D	101163	1

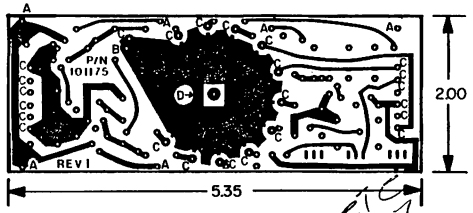
SHEET 1 OF 1

SYMBOL	DESCRIPTION	QTY
UNMARKED	.035 DIA.	91
A	.052 DIA.	6
B	.098 DIA.	11
C	.063 DIA.	24
D	.50 DIA.	1

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENGINEERING RELEASE	2097	10-31-79 DS	11-1-79

NOTES:

1. ALL HOLES LOCATED ON .050 GRID WITHIN .005 OF THEIR TRUE POSITION UNLESS OTHERWISE SPECIFIED.
2. ALL HOLES SHALL BE PLATED THRU WITH A MINIMUM OF .001 INCH THICK COPPER.
3. FINISHED HOLE SIZE SHALL BE ± .003 OF NORMAL HOLE SIZE AFTER PLATING, WITH A MINIMUM ANNULAR RING OF .010.
4. CONNECTOR CONTACTS SHALL BE PLATED WITH GOLD OVER LOW STRESS NICKEL. GOLD PLATING SHALL BE A MINIMUM OF .00005 INCH THICK AND SHALL BE IN ACCORDANCE WITH MIL-G-45204. LOW STRESS NICKEL PLATING. SHALL BE A MINIMUM OF .0005 INCH THICK.
5. FINISH SHALL BE COPPER (EXCEPT CONNECTOR CONTACTS) PLATED WITH ELECTRODEPOSITED TIN-LEAD. PLATING SHALL BE A MINIMUM OF .0003 INCH THICK AND SHALL BE 60% ± 10% TIN.
6. MATERIAL SHALL BE FR-4 IN ACCORDANCE WITH MIL-P-13949.
7. SILKSCREEN NOMENCLATURE ON COMPONENT SIDE WITH NONCONDUCTIVE WHITE INK.
8. SOLDER MASK SHALL BE PROVIDED ON CIRCUIT SIDE (BACK) USING COLONIAL INK ER 7040 GREEN SOLDER MASK OR EQUIVALENT. LEAVE ALL PADS UNMASKED.



OBSOLETE
PER ECN 2417
GEB 3-3-83

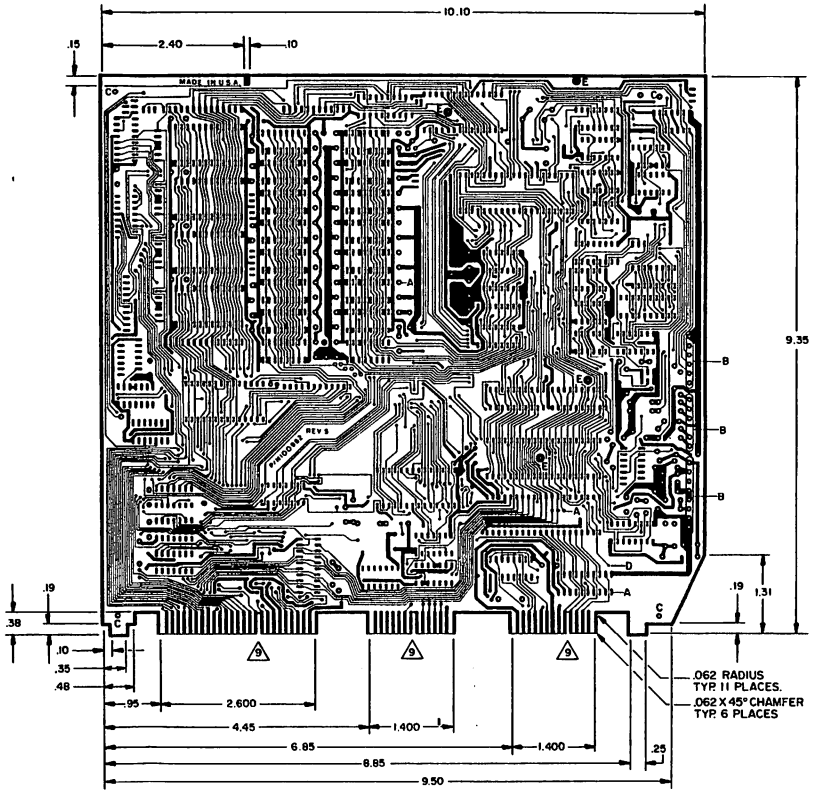
APPROVALS	DATE	Intelligent Systems Corp. ®	
STEPHENS, D	9-7-79	DRILL DRAWING VIDEO PCB (3000 SERIES)	
		SIZE C	CODE IDENT NO
		DRAWING NO 101175	REV 1
		SCALE FULL	SHEET 1 OF 1

DECIMALS .015 .005
MATERIAL
FINISH
NEXT ASSY USED ON
APPLICATION
DO NOT SCALE DRAWING

5 4 3 2 1

A B C

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
5	SEE ECN	2638	8-27-82	



NOTES:

1. ALL HOLES LOCATED ON .050 GRID WITHIN .005 OF THEIR TRUE POSITION UNLESS OTHERWISE SPECIFIED.
2. ALL HOLES SHALL BE PLATED THRU WITH A MINIMUM OF .001 INCH THICK COPPER.
3. FINISHED HOLE SIZE SHALL BE ± .003 OF NORMAL HOLE SIZE AFTER PLATING, WITH A MINIMUM ANNULAR RING OF .010.
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⑨ .050 X .38 NOTCH 3 PLACES.

SYMBOL	DESCRIPTION	QTY
UNMARKED		
A	.035 DIA.	1563
B	.052 DIA.	19
C	.140 DIA.	4
D	.028 DIA.	461
E	.156 DIA. UNPLATED	4

QTY REQD	SYM IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

APPROVALS	DATE	Intelligent Systems Corp.
DRAWN TAYLOR	3/22/82	DRILL DRAWING DIGITAL BOARD
CHECKED		

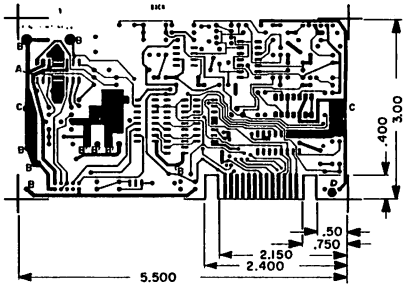
SIZE	CODE IDENT NO	DRAWING NO	REV
D		100962-25	5

SCALE | SHEET 1 OF 1

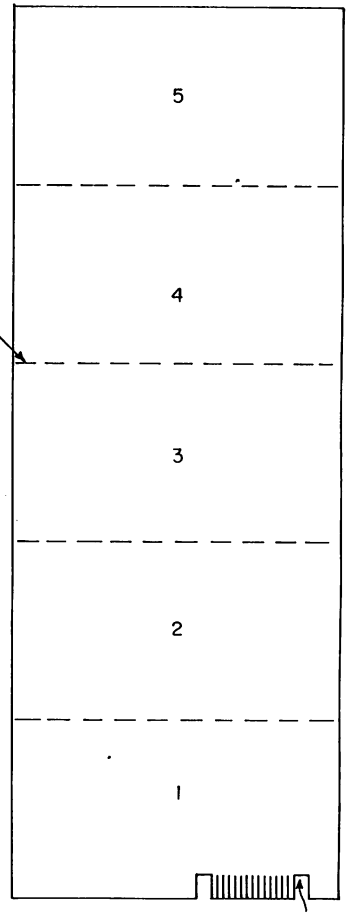
MATERIAL | FINISH | NEXT ASSY | USED ON | APPLICATION | DO NOT SCALE DRAWING

TOLERANCES UNLESS OTHERWISE SPECIFIED: FRACTIONS .015, DECIMALS .XX .015, .XXX .005, ANGLES 1°

REV	ZONE	LTR	REVISION	DATE	APPROVED
6			REVISED AND REDRAWN	11-14-78	



DETAIL "A"



DOTTED LINES TO BE SCORED FOR BREAKAWAY

CUT OUT APPLIES TO BOARD "1 ONLY SEE DETAIL "A"

NOTES:

1. ALL HOLES LOCATED ON .050 GRID WITHIN .005 OF THEIR TRUE POSITION UNLESS OTHERWISE SPECIFIED.
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6. MATERIAL SHALL BE FR-4 IN ACCORDANCE WITH MIL-P-13949.
7. SILKSCREEN NOMENCLATURE ON COMPONENT SIDE WITH NONCONDUCTIVE WHITE INK.

SYMBOL	DESCRIPTION	QTY
UNMARKED	.031 - .036	321
A	.040 X .166	2
B	.051 - .056	9
C	.139 - .145	2
D	.061 - .066	1

PARTS LIST

.062 THICK

DO NOT SCALE DRAWING

K. J. H

11-14-78

Intelligent Systems Corp.®

DRILL DRAWING

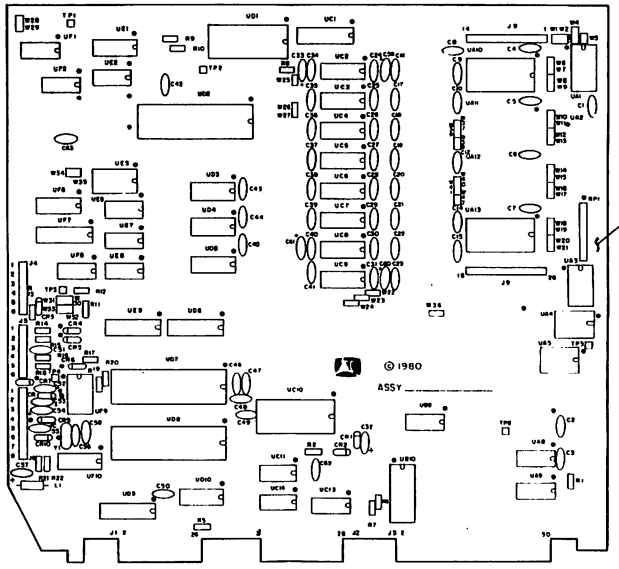
DISK CONTROLLER

SIZE	TODD IDENT NO	DRAWING NO	REV
D		100871 26	6

SCALE

SHEET OF

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	2638	4-22-82	



2

APPROVALS	DATE
DRAWN JEB	4/22/82
CHECKED	
ENG	

FOR REV. 5 PCB

FINISH

DO NOT SCALE DRAWING

PROPRIETARY

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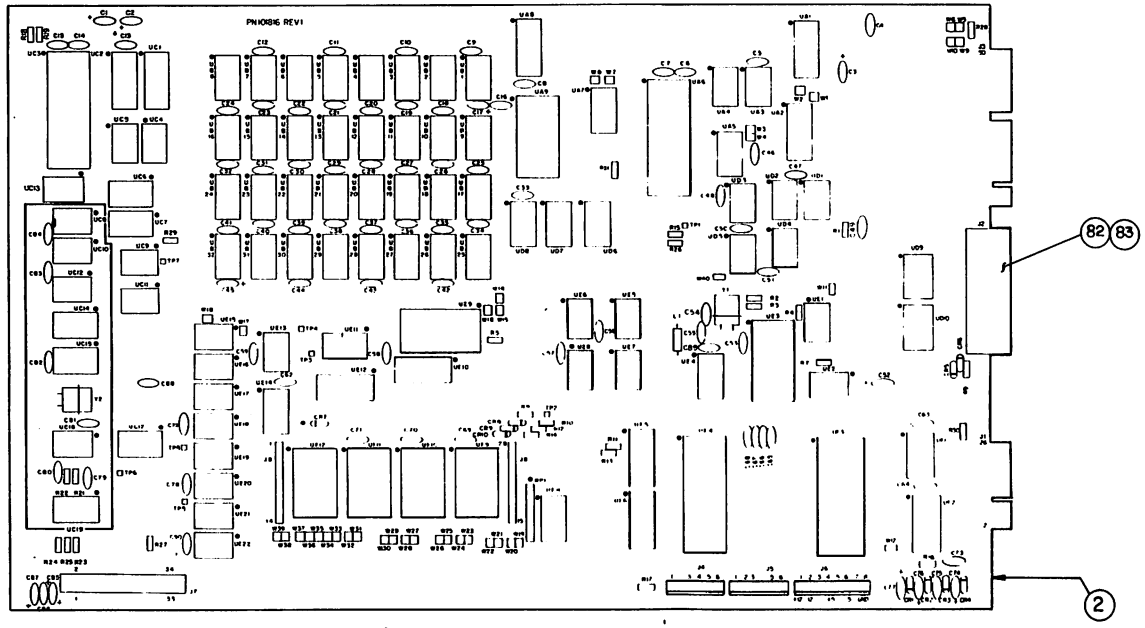
Intelligent Systems

PCB ASSEMBLY
SINGLE BOARD LOGIC - B
2048

SIZE D | DRAWING NO 101944 | REV 1

SCALE | SHEET | OF

P/L LEVEL				REV	DESCRIPTION	ECN	DATE	APPROVED
817	818	819	820					
1	1	1	1	1	ENG. RELEASE	2435	6-16-81	
2	2	2	2	2	SEE ECN	2621	3-19-82	
3	3	3	3	3	REMOVE SOCKETS	2682	5-28-82	
4	4	4	4	4	SEE ECN	2733	7-15-82	



NOTES:

*1. SEE REVISION BLOCK FOR REVISION LEVEL OF INDIVIDUAL PART NUMBERS.

APPROVALS	DATE
DRAWN RLC	9-16-81
CHECKED	
ENG	

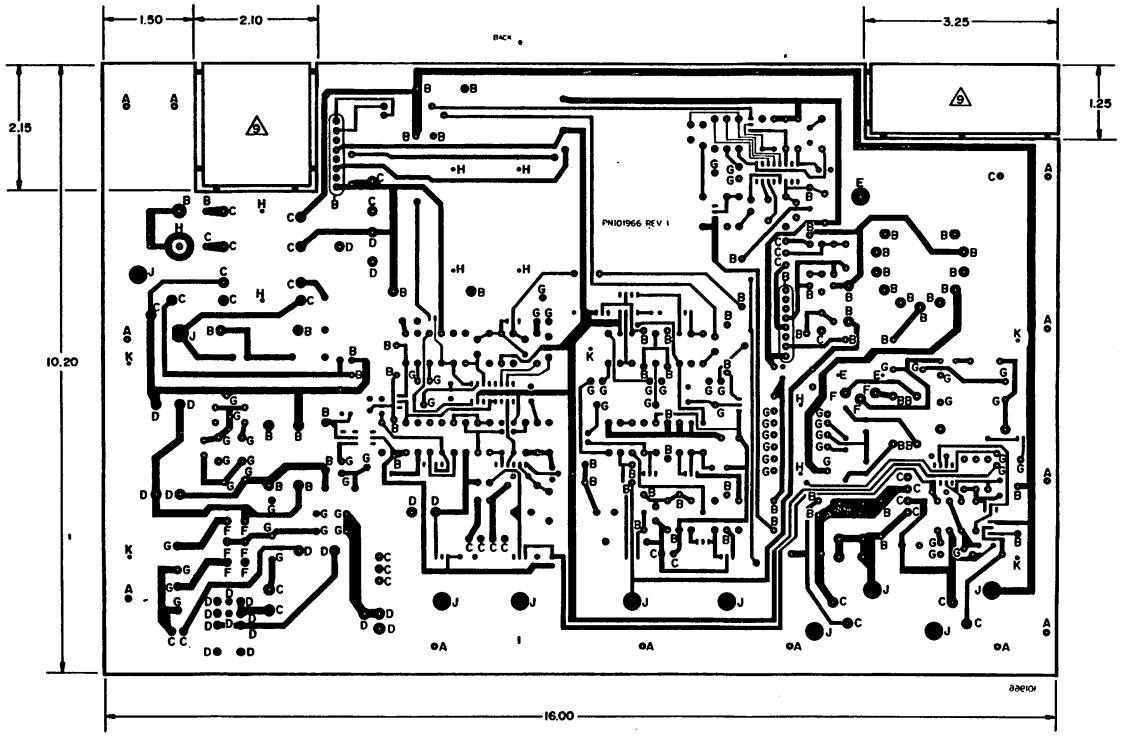
PROPRIETARY

Intelligent Systems

PCB ASSEMBLY
3650 SERIES LOGIC
WITH IMAGE RESOURCE

SIZE D | DRAWING NO 101817, 18, 19, 20* 2 of | REV 4

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED



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⑨ TO BE ROUTED WITH 1/8" BIT LEAVING ELEVEN TABS APPROX. 1/8" AS SHOWN.

SYMBOL	DESCRIPTION	QTY
UNMARKED	.035 DIA.	198
A	.140 DIA.	12
B	.056 DIA.	89
C	.065 DIA.	38
D	.075 DIA.	21
E	.100 DIA.	3
F	.090 DIA.	9
G	.046 DIA.	64
H	.200 UNPLATED	9
J	.155 DIA.	10
K	.140 UNPLATED	5

NEXT ASSY | USED ON

APPLICATION

QTY REQD | ITEM IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .015 ± 1° .XXX ± .005

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN TAYLOR	7/6/82
CHECKED	

FOR REV IP4 PCB

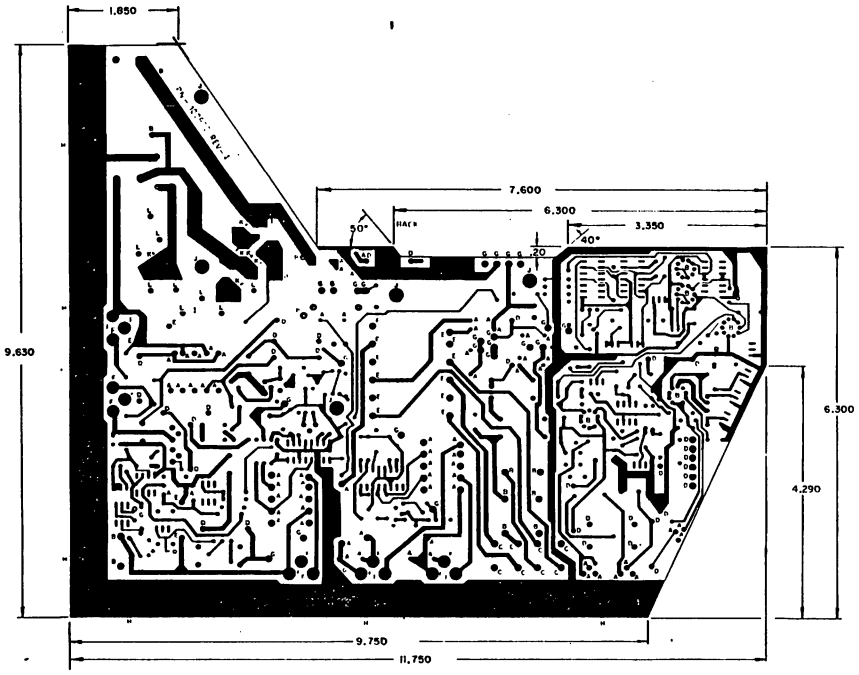
Intelligent Systems Corp.®

DRILL DRAWING
LCCT ANALOG
2400 SERIES

SIZE D | CODE IDENT NO | DRAWING NO 101966 29 | REV IP5

SCALE | SHEET 1 OF 1

REV			ECN	DATE	APPROVED
4		REVISED AND REDRAWN	N18279		
4A	C4	CHG 2 HOLES FM UNMKD TO G	2205	NH1-21-80	



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SYMBOL	DESCRIPTION	QTY
UNMARKED	.032-.037	
A	.037-.042	68
B	.040-.045	62
C	.046-.050	8
D	.051-.056	36
E	.058-.063	16
F	.069-.074	15
G	.072-.077	25
H	.139-.145	6
J	.249-.255 (UNPLATED)	5
K	.274-.280	6
L	.370-.376 (UNPLATED)	9

Intelligent Systems Corp.

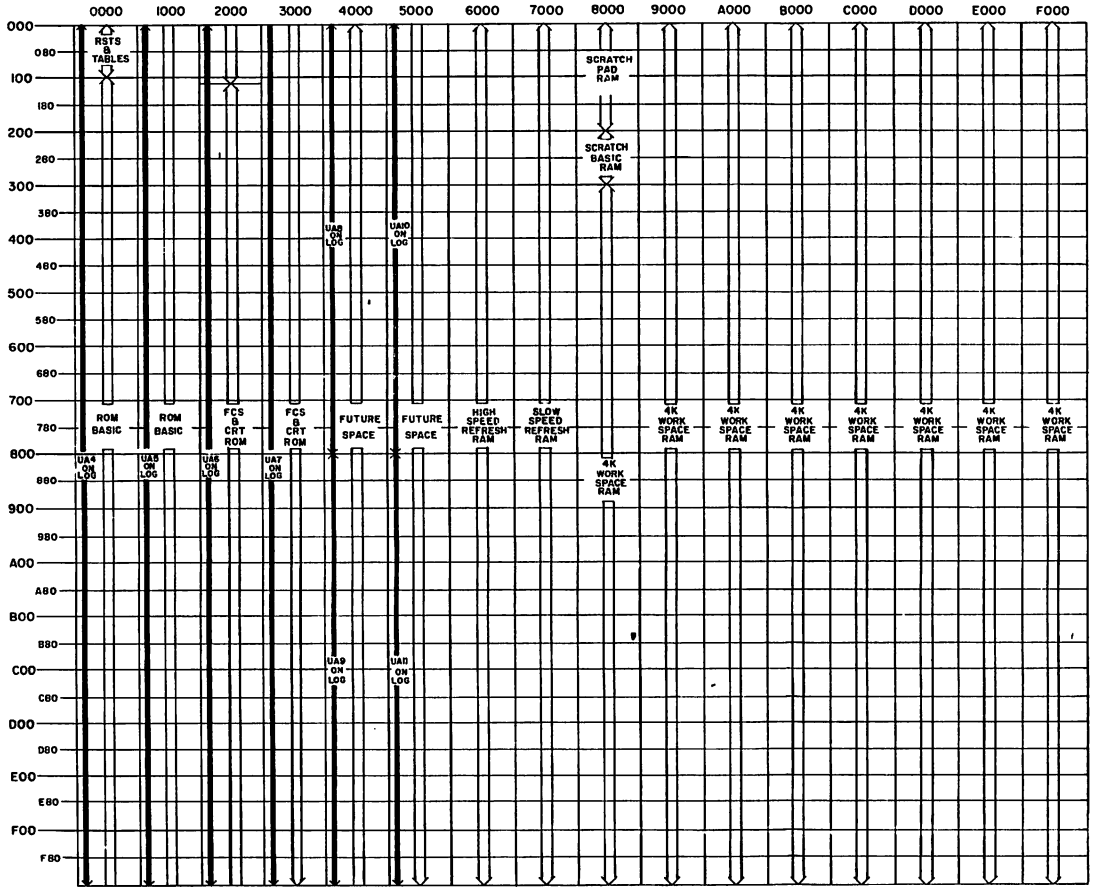
DRILL DRAWING

CC II ANALOG

D 100900 REV 4A

SHEET 1/1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	1	REDRAWN	8-16-78	



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.X ±
.XX ±
.XXX ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN H E Harris	8-16-78
CHECKED Stanley Hazard	9-11-78

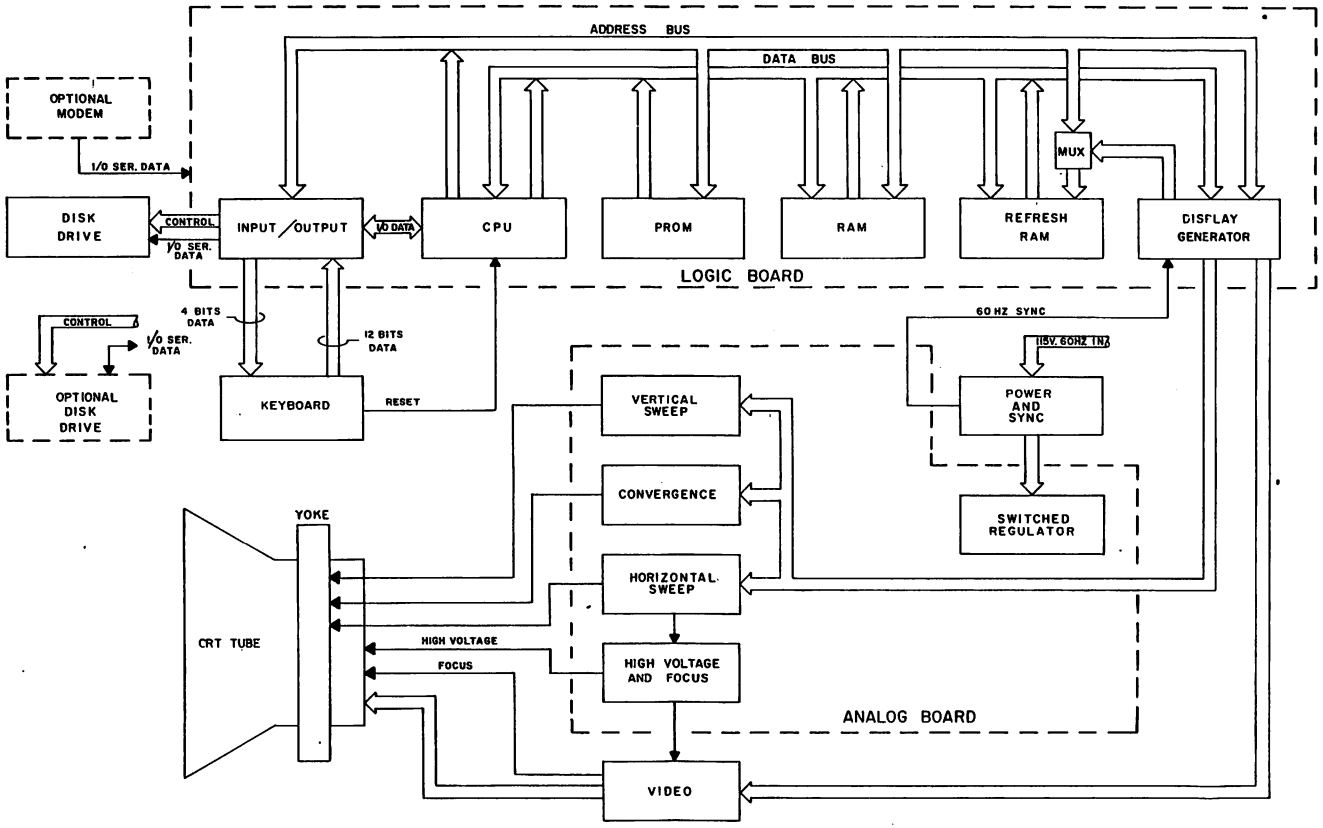
Intelligent Systems Corp.®

MEMORY MAP COMPUCOLOR II

SIZE	CODE IDENT NO	DRAWING NO	REV
D		100991	1

SCALE | SHEET 31 OF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX
XXX

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN	5-2-78
CHECKED	7-12-78

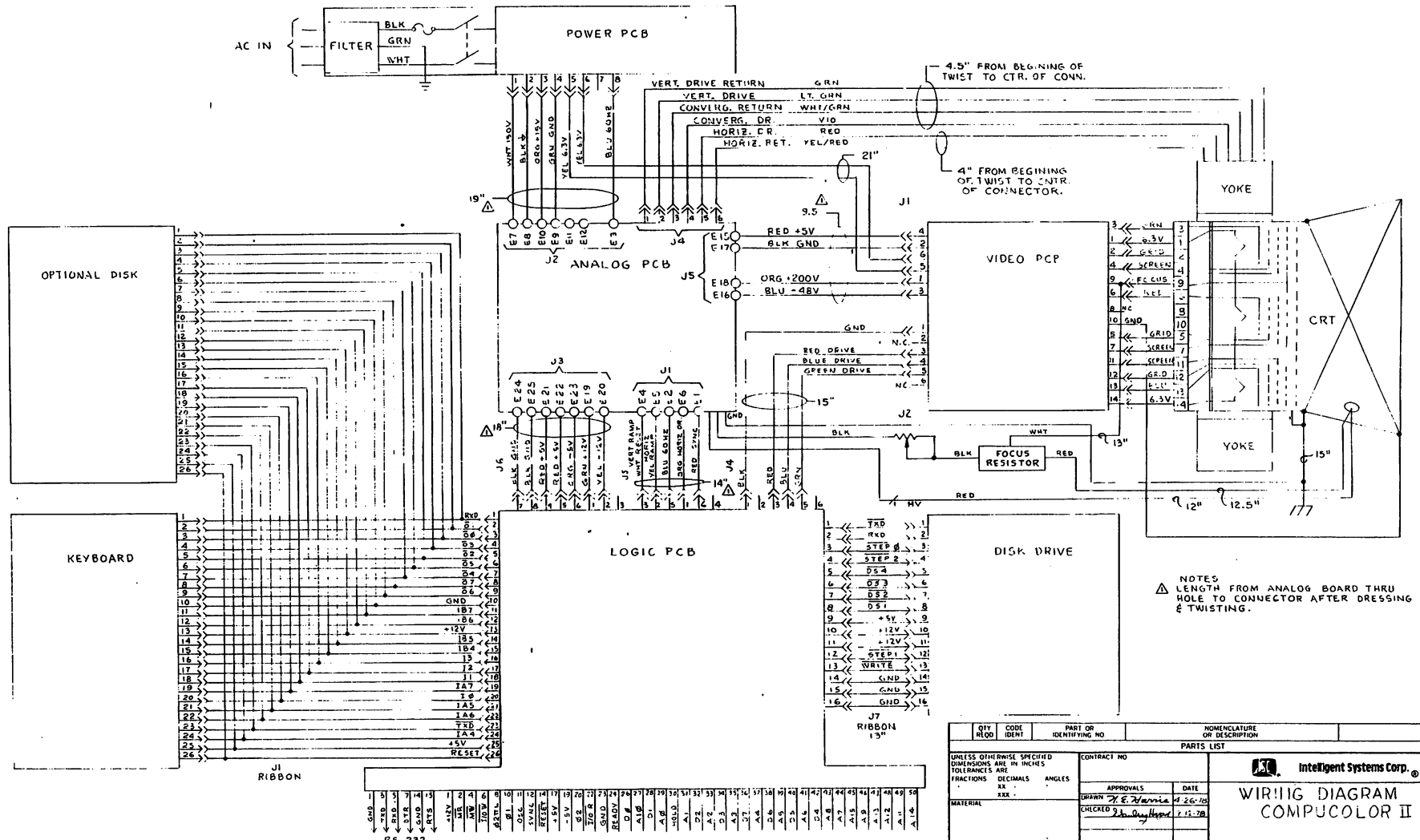
Intelligent Systems Corp.®

COMPUCOLOR II BLOCK DIAGRAM

SIZE	CODE IDENT NO	DRAWING NO
D		100995

SCALE — | SHEET 1 OF 1

32



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX .
.XXX .

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN T. E. Harris	4-26-78
CHECKED D. L. Quyllen	5-12-78

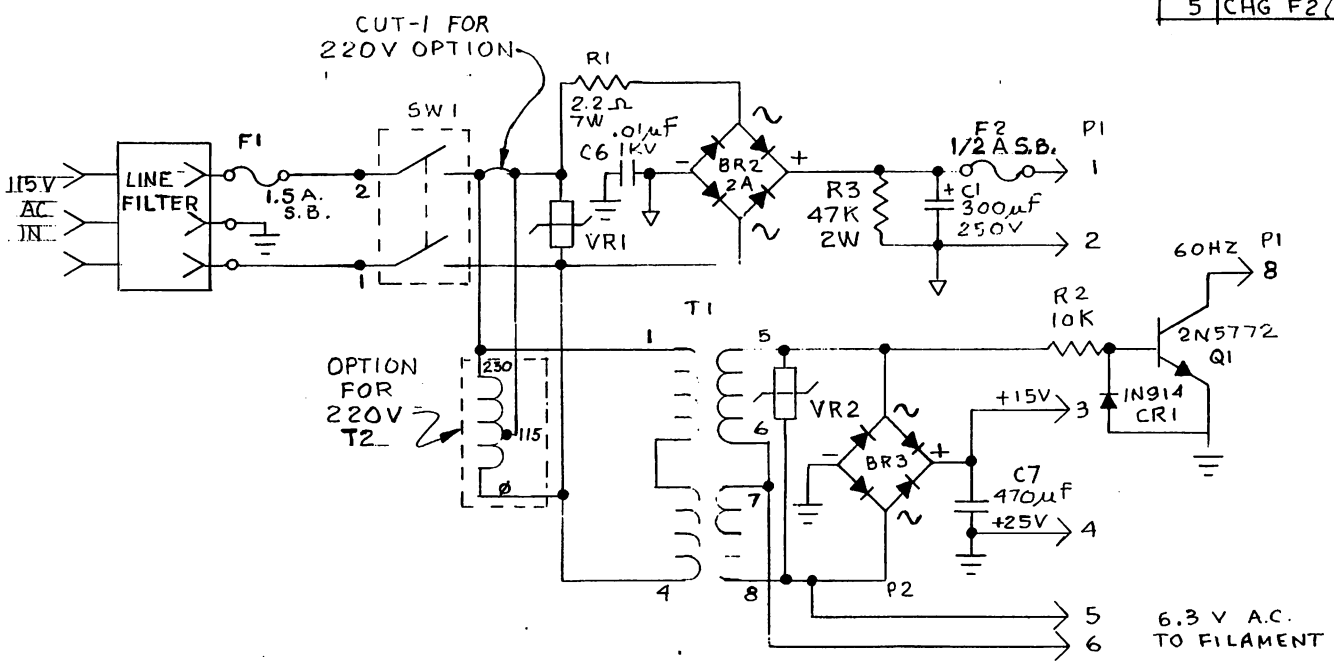
Intelligent Systems Corp.

WIRING DIAGRAM COMPUCOLOR II

SIZE	CODE IDENT NO	DRAWING NO	REV.
D		100990	32

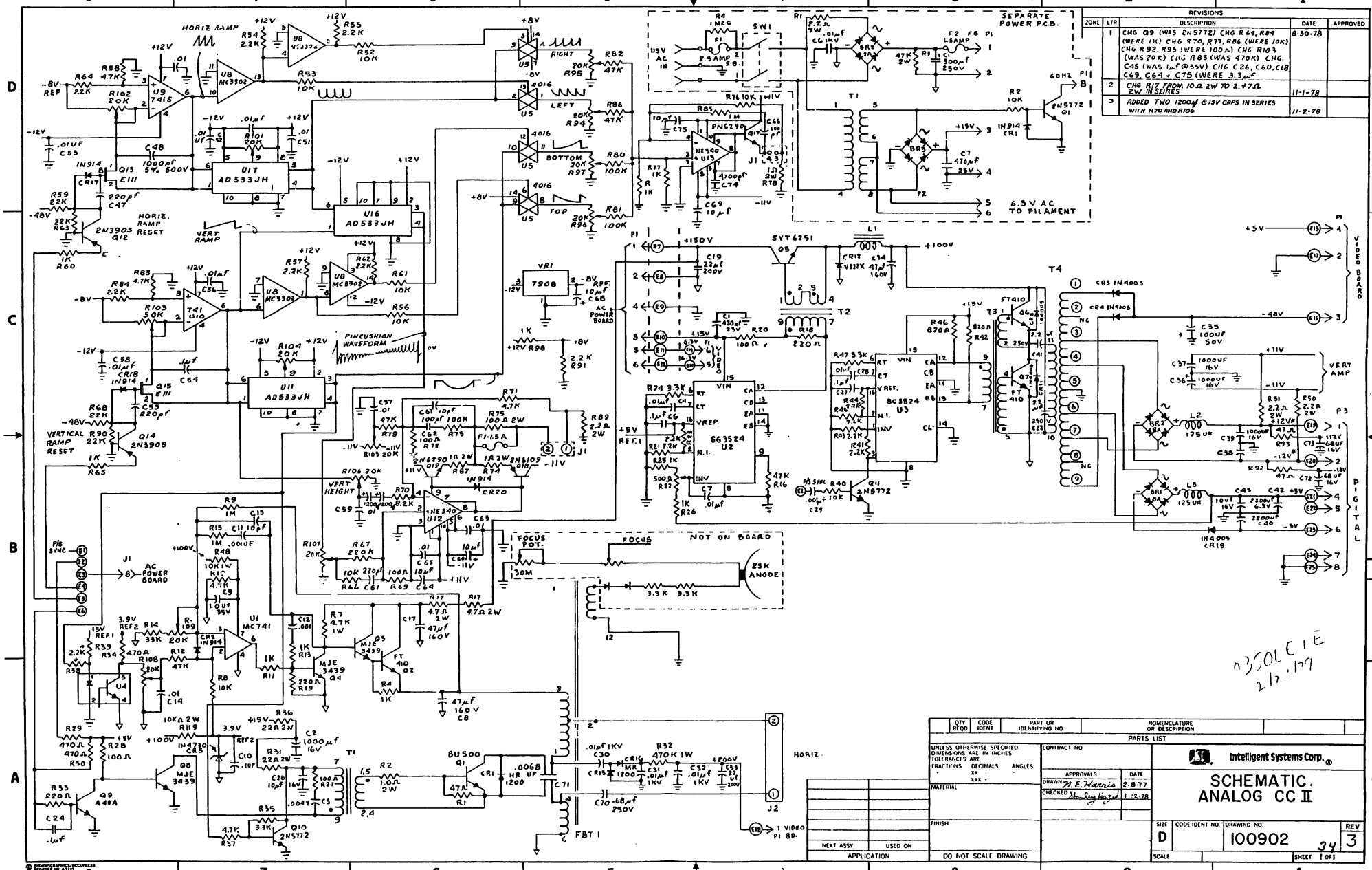
SCALE | SHEET OF

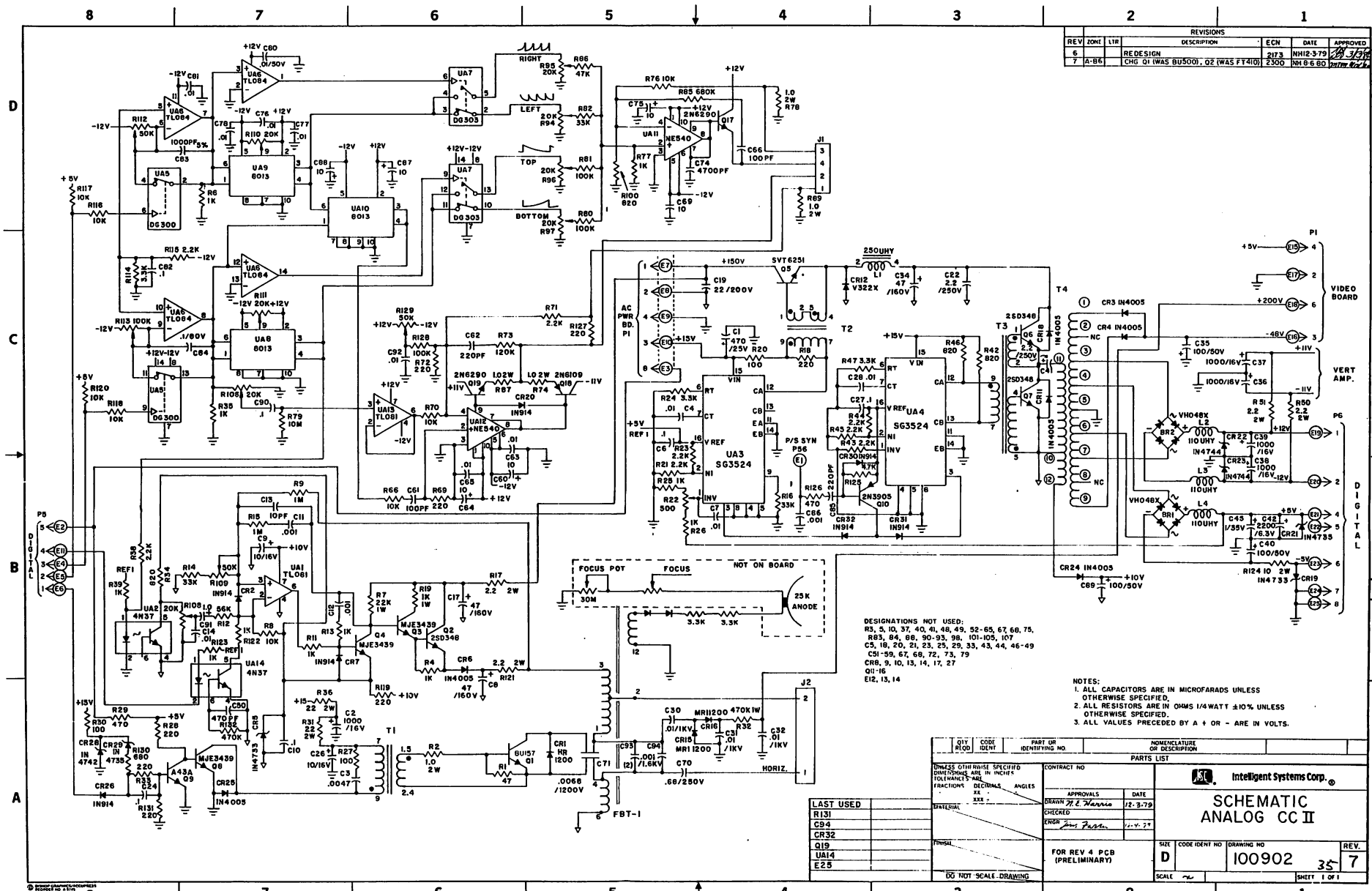
REV.	DESCRIPTION	DATE	APPROVED
1	ADD VR1 AHEAD OF SW1 BY N.E.H.	10-12-78	
2	MOVE VR1 AFTER SW1 ADD VR2 SHOW LINE FILTER BY N.E.H.	10-16-78	
3	PROVIDE FOR 220V OPS., ADD T2	12-8-78	
4	CHG F2 (WAS 1.5AMP) ECN 2051	3/16/79 NH	3-22-79
5	CHG F2 (WAS 3/4 AMP) ECN 2192	12/5/79 NH	12/10/79

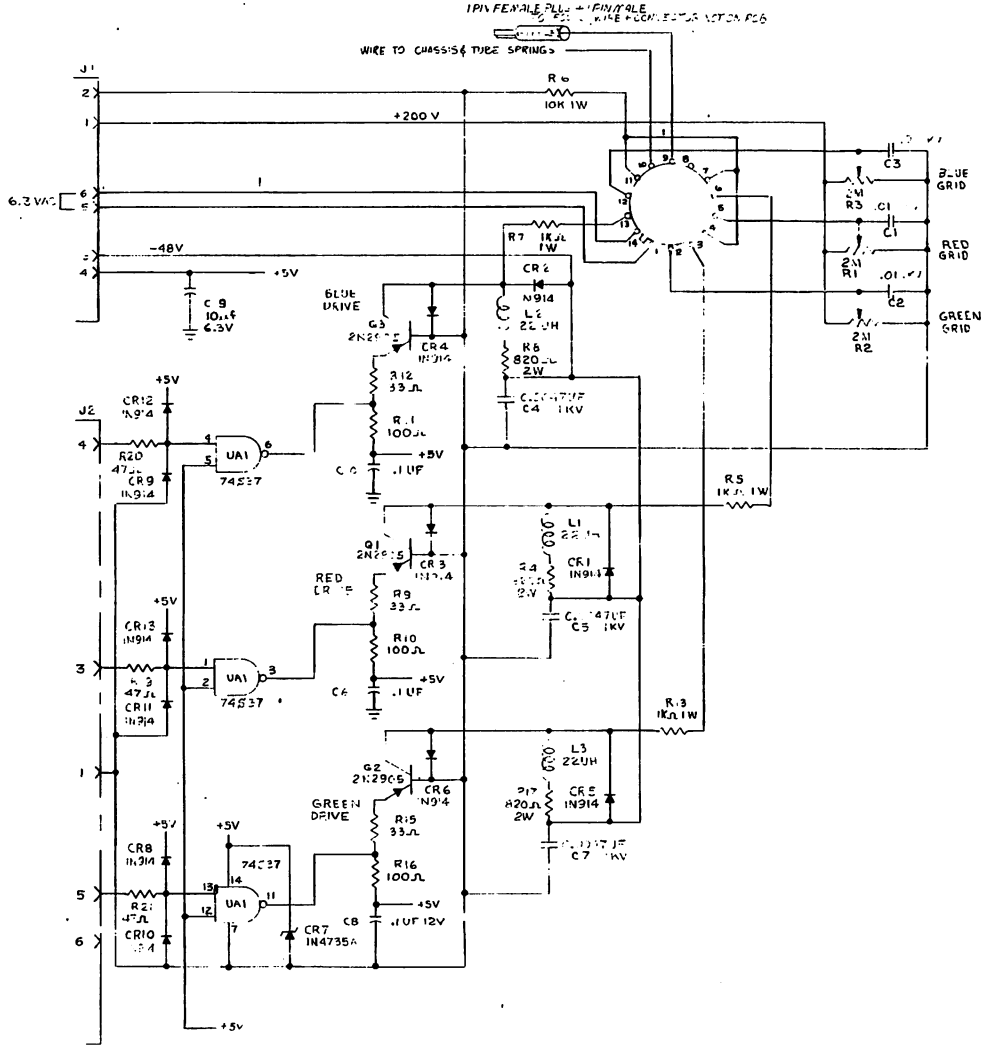


Intelligent Systems Corp.			
SCALE: ~	APPROVED BY:	DRAWN BY N.E.H.	
DATE: 2-8-78		REVISED 10.12.78	
SCHEMATIC A/C PWR. SUPPLY C/C II			
33		DRAWING NUMBER 100903	REV 5

11X17 PRINTED ON NO. 1000H CLEARPRINT


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
1 | CHG Q9 (WAS 2N5772) CHG R69, R89 (WERE 1K) CHG R70, R77, R86 (WERE 10K) CHG R92, R93 (WERE 100Ω) CHG R103 (WAS 20K) CHG R85 (WAS 470K) CHG. C45 (WAS 1μF @35V) CHG C26, C60, C68 C69, C64 & C75 (WERE 3.3μF | 8-30-78
2 | CHG R17 FROM 10Ω 2W TO 2.7Ω 2W IN SERIES | 11-1-78
3 | ADDED TWO 1200μF 6.3V CAPS IN SERIES WITH R70 AND R106 | 11-2-78
SEPARATE POWER P.C.B.
6.3 V AC TO FILAMENT
HORIZ RAMP
VERT. RAMP
HORIZ. RAMP RESET
VERT. RAMP RESET
PINCUSHION WAVEFORM
VERT HEIGHT
FOCUS POT.
NOT ON BOARD
FOCUS
25K ANODE
AC POWER BOARD
VIDEO BOARD
DIGITAL
VERT AMP
HORIZ
FBT 1
OBSOLETE 2-12-79
PARTS LIST
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ±.01 .XXX ±.005
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS | DATE
DRAWN M. E. Harris 2-8-77
CHECKED 1-12-78
Intelligent Systems Corp.
SCHEMATIC. ANALOG CC II
SIZE D | CODE IDENT NO | DRAWING NO. 100902 | REV 3
SCALE | SHEET 1 OF 1


REVISIONS
REV | ZONE | LTR | DESCRIPTION | ECN | DATE | APPROVED
6 | | | RE DESIGN | 2173 | NH 12-3-79 |
7 | A-86 | | CHG Q1 (WAS BU500), Q2 (WAS FT410) | 2300 | NH 8-6-80 |
DESIGNATIONS NOT USED:
R3, 5, 10, 37, 40, 41, 48, 49, 52-65, 67, 68, 75, R83, 84, 88, 90-93, 98, 101-105, 107
C5, 18, 20, 21, 23, 25, 29, 33, 43, 44, 46-49
C51-59, 67, 68, 72, 73, 79
CR8, 9, 10, 13, 14, 17, 27
Q11-16
E12, 13, 14
NOTES:
1. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE IN OHMS 1/4 WATT ±10% UNLESS OTHERWISE SPECIFIED.
3. ALL VALUES PRECEDED BY A + OR - ARE IN VOLTS.
PARTS LIST
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION
LAST USED
R131
C94
CR32
Q19
UA14
E25
Intelligent Systems Corp.
SCHEMATIC
ANALOG CC II
FOR REV 4 PCB
(PRELIMINARY)
SIZE D | CODE IDENT NO | DRAWING NO 100902 | REV. 7
SCALE ~ | SHEET 1 OF 1
DO NOT SCALE DRAWING
DRAWN M. E. Harris 12-3-79
CHECKED
ENGR Jim Peterson 12-4-79
VIDEO BOARD
VERT AMP.
DIGITAL
FOCUS POT
FOCUS
NOT ON BOARD
25K ANODE
30M
3.3K
3.3K
AC PWR BD. P1
FBT-1
HORIZ.
REF1
REF I
+5V REF I
P/S SYN P56
SG3524
UA3
UA4
T1
T2
T3
T4
L1
L2
L4
L5
J1
J2
P1
P5
P6



REV	ZONE	LTR	DESCRIPTION	DATE	APPROVED
1			REDESIGNED JMS 2-21-78		
2			CHG J1 CONNS, DELETE LEED	5-17-78	
3			REDESIGNED	6-27-78	
4			CHG R23 (WAS 1KΩ) CHG R6, 12, 16 (WERE 47Ω) CHG C18 (WAS 6.8μF) DELETE R22, C5, 7, 10, 12, 15, 17 & 20) ADD R8, 14 & 20 BY N.E.H.	9-18-78	
5			REDESIGN BY N.E.H.	10-18-78	
6			DELETED R19, 19	10-31-78	
7	2059		CHG R5, R7 R13 FROM 470 ~2W TO 1K Ω 1W		

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX
XXX

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

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APPENDICES

APPENDIX A

TMS 8080 Microprocessor

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LIST OF ILLUSTRATIONS

TMS 8080 MICROPROCESSOR

1. ARCHITECTURE

1.1 INTRODUCTION

The TMS 8080 is an 8-bit parallel central processing unit (CPU) fabricated on a single chip using a high-speed N-channel silicon-gate process. (See Figure 1). A complete microcomputer system with a 2-μs instruction cycle can be formed by interfacing this circuit with any appropriate memory. Separate 8-bit data and 16-bit address buses simplify the interface and allow direct addressing of 65,536 bytes of memory. Up to 256 input and 256 output ports are also provided with direct addressing. Control signals are brought directly out of the processor and all signals, excluding clocks, are TTL compatible.

1.2 THE STACK

The TMS 8080 incorporates a stack architecture in which a portion of external memory is used as a pushdown stack for storing data from working registers and internal machine status. A 16-bit stack pointer (SP) is provided to facilitate stack location in the memory and to allow almost unlimited interrupt handling capability. The CALL and RST (restart) instructions use the SP to store the program counter (PC) into the stack. The RET (return) instruction uses the SP to acquire the previous PC value. Additional instructions allow data from registers and flags to be saved in the stack.

1.3 REGISTERS

The TMS 8080 has three categories of registers: general registers, program control registers, and internal registers. The general registers and program control registers are listed in Table 1. The internal registers are not accessible by the programmer. They include the instruction register, which holds the present instruction, and several temporary storage registers to hold internal data or latch input and output addresses and data.

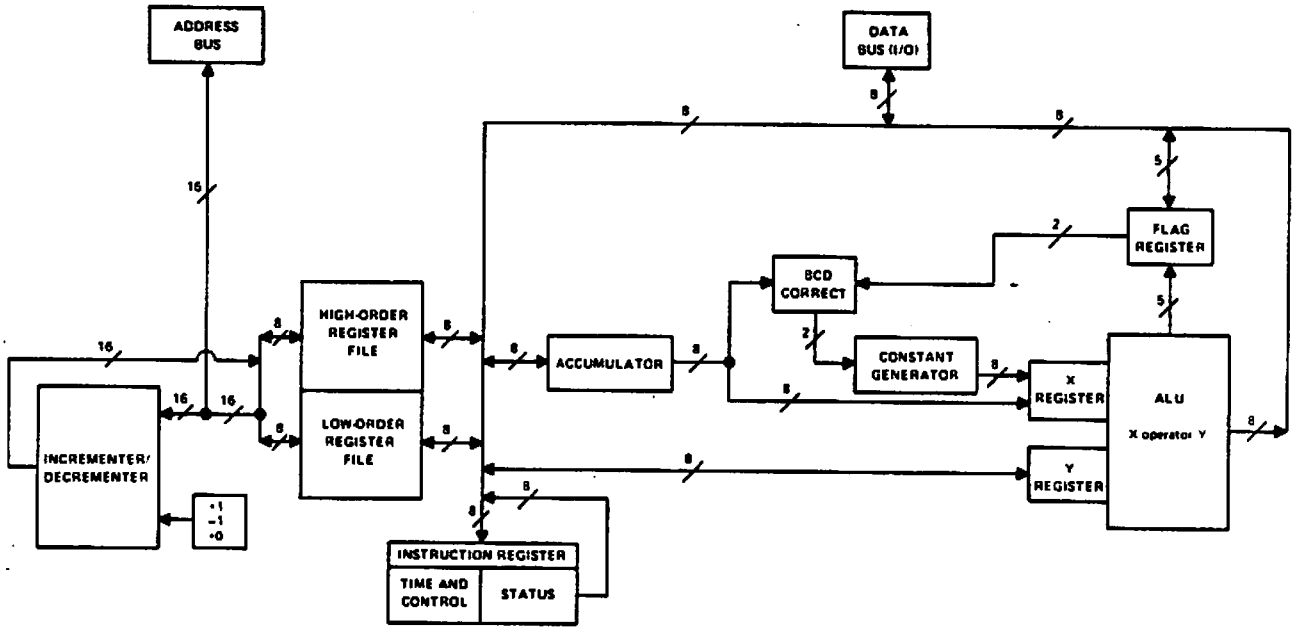


FIGURE 1–TMS 8080 FUNCTIONAL BLOCK DIAGRAM

1.4 THE ARITHMETIC UNIT

Arithmetic operations are performed in an 8-bit parallel arithmetic unit that has both binary and decimal capabilities. Four testable internal flag bits are provided to facilitate program control, and a fifth flag is used for decimal corrections. Table 2 defines these flags and their operation. Decimal corrections are performed with the DAA instruction. The DAA corrects the result of binary arithmetic operation on BCD data as shown in Table 3.

1.5 STATUS AND CONTROL

Two types of status are provided by the TMS8080. Certain status is indicated by dedicated control lines. Additional status is transmitted on the data bus during the beginning of each instruction cycle (machine cycle). Table 4 indicates the pin functions of the TMS8080. Table 5 defines the status information that is presented during the beginning of each machine cycle (SYNC time) on the data bus.

1.6 I/O OPERATIONS

Input/output operations (I/O) are performed using the IN and OUT instructions. The second byte of these instructions indicates the device address (256 device addresses). When an IN instruction is executed, the input device address appears in duplicate on A7 through A0 and A15 through A8, along with $\overline{WO}$ and INP status on the data bus. The addressed input device then puts its input data on the data bus for entry into the accumulator. When an OUT instruction is executed, the same operation occurs except that the data bus has OUT status and then has output data.

Direct memory access channels (DMA) can be OR-tied directly with the data and address buses through the use of the HOLD and HLDA (hold acknowledge) controls. When a HOLD request is accepted by the CPU, HLDA goes high, the address and data lines are forced to a high-impedance or "floating" condition, and the CPU stops until the HOLD request is removed.

Interfacing with different speed memories is easily accomplished by use of the WAIT and READY pins. During each machine cycle, the CPU polls the READY input and enters a wait condition until the READY line becomes true. When the WAIT output pin is high, it indicates that the CPU has entered the wait state.

Designing interrupt driven systems is simplified through the use of vectored interrupts. At the end of each instruction, the CPU polls the INT input to determine if an interrupt request is being made. This action does not occur if the CPU is in the HOLD state or if interrupts are disabled. The INTE output indicates if the interrupt logic is enabled (INTE is high). When a request is honored, the INTA status bit becomes high, and an RST instruction may be inserted to force the CPU to jump to one of eight possible locations. Enabling or disabling interrupts is controlled by special instructions (EI or DI). The interrupt input is automatically disabled when an interrupt request is accepted or when a RESET signal is received.

1.7 INSTRUCTION TIMING

The execution time of the instructions varies depending on the operation required and the number of memory references needed. A machine cycle is defined to be a memory referencing operation and is either 3, 4, or 5 state times long. A state time (designated S) is a full cycle of clocks $\phi 1$ and $\phi 2$. (NOTE: The exception to this rule is the DAD instruction, which consists of 1 memory reference in 10 state times). The first machine cycle (designated M1) is either 4 or 5 state times long and is the "instruction fetch" cycle with the program counter appearing on the address bus. The CPU then continues with as many M cycles as necessary to complete the execution of the instruction (up to a maximum of 5). Thus the instruction execution time varies from 4 state times (several including ADDr) to 18 (XTHL). The WAIT or HOLD conditions may affect the execution time since they can be used to control the machine (for example to "single step") and the HALT instruction forces the CPU to stop until an interrupt is received. As the instruction execution is completed (or in the HALT state) the INT pin is polled for an interrupt. In the event of an interrupt, the PC will not be incremented during the next M1 and an RST instruction can be inserted.

TABLE 1
TMS 8080 REGISTERS

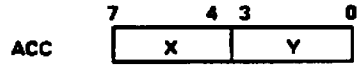
NAME	DESIGNATOR	LENGTH	PURPOSE
Accumulator	A	8	Used for arithmetic, logical, and I/O operations
B Register	B	8	General or most significant 8 bits of double register BC
C Register	C	8	General or least significant 8 bits of double register BC
D Register	D	8	General or most significant 8 bits of double register DE
E Register	E	8	General or least significant 8 bits of double register DE
H Register	H	8	General or most significant 8 bits of double register HL
L Register	L	8	General or least significant 8 bits of double register HL
Program Counter	PC	16	Contains address of next byte to be fetched
Stack Pointer	SP	16	Contains address of the last byte of data saved in the memory stack
Flag Register	F	5	Five flags (C, Z, S, P, C1)

NOTE: Registers B and C may be used together as a single 16-bit register, likewise, D and E, and H and L.

TABLE 2
FLAG DESCRIPTIONS

SYMBOL	TESTABLE	DESCRIPTION
C	YES	C is the carry/borrow out of the MSB (most significant bit) of the ALU (Arithment Logic Unit). A TRUE condition (C = 1) indicates overflow for addition or underflow for subtraction.
Z	YES	A TRUE condition (Z = 1) indicates that the output of the ALU is equal to zero.
S	YES	A TRUE condition (S = 1) indicates that the MSB of the ALU output is equal to a one (1).
P	YES	A TRUE condition (P = 1) indicates that the output of the ALU has even parity (the number of bits equal to one is even).
C1	NO	C1 is the carry out of the fourth bit of the ALU (TRUE condition). C1 is used only for BCD correction with the DAA instruction.

TABLE 3
FUNCTION OF THE DAA INSTRUCTION
Assume the accumulator (A) contains two BCD digits, X and Y



ACCUMULATOR BEFORE DAA				ACCUMULATOR AFTER DAA			
C	$A_7 \ldots A_4$	C1	$A_3 \ldots A_0$	C	$A_7 \ldots A_4$	C1	$A_3 \ldots A_0$
0	X < 10	0	Y < 10	0	X	0	Y
0	X < 10	1	Y < 10	0	X	0	Y + 6
0	X < 9	0	Y > 10	0	X + 1	1	Y + 6
1	X < 10	0	Y < 10	1	X + 6	0	Y
1	X < 10	1	Y < 10	1	X + 6	0	Y + 6
1	X < 10	0	Y ≥ 10	1	X + 7	1	Y + 6
0	X ≥ 10	0	Y < 10	1	X + 6	0	Y
0	X > 10	1	Y < 10	1	X + 6	0	Y + 6
0	X ≥ 9	0	Y ≥ 10	1	X + 7	1	Y + 6

NOTE: The corrections shown in Table 3 are sufficient for addition. For subtraction, the programmer must account for the borrow condition that can occur and give erroneous results. The most straight forward method is to set A = 99_{16} and carry = 1. Then add the minuend to A after subtracting the subtrahend from A.

TABLE 4
TMS 8080 PIN DEFINITIONS

SIGNATURE	PIN	I/O	DESCRIPTION
A15 (MSB)	36	OUT	A15 through A0 comprise the address bus. True memory or I/O device addresses appear on this 3-state bus during the first state time of each instruction cycle.
A14	39	OUT	
A13	38	OUT	
A12	37	OUT	
A11	40	OUT	
A10	1	OUT	
A9	35	OUT	
A8	34	OUT	
A7	33	OUT	
A6	32	OUT	
A5	31	OUT	
A4	30	OUT	
A3	29	OUT	
A2	27	OUT	
A1	26	OUT	
A0 (LSB)	25	OUT	
D7 (MSB)	6	IN/OUT	D7 through D0 comprise the bidirectional 3-state data bus. Memory, status, or I/O data is transferred on this bus.
D6	5	IN/OUT	
D5	4	IN/OUT	
D4	3	IN/OUT	
D3	7	IN/OUT	
D2	8	IN/OUT	
D1	9	IN/OUT	
D0 (LSB)	10	IN/OUT	
V_{SS}	2		Ground reference
V_{BB}	11		Supply voltage (−5 V nominal)
V_{CC}	20		Supply voltage (5 V nominal)
V_{DD}	28		Supply voltage (12 V nominal)
$\phi 1$	22	IN	Phase 1 clock.
$\phi 2$	15	IN	Phase 2 clock. See page 19 for $\phi 1$ and $\phi 2$ timing.
RESET	12	IN	Reset. When active (high) for a minimum of 3 clock cycles, the RESET input causes the TMS 8080 to be reset. PC is cleared, interrupts are disabled, and after RESET, instruction execution starts at memory location 0. To prevent a lockup condition, a HALT instruction must not be used in location 0.
HOLD	13	IN	Hold signal. When active (high) HOLD causes the TMS 8080 to enter a hold state and float (put the 3-state address and data bus in a high-impedance state). The chip acknowledges entering the hold state with the HLDA signal and will not accept interrupts until it leaves the hold state.
INT	14	IN	Interrupt request. When active (high) INT indicates to the TMS8080 that an interrupt is being requested. The TMS8080 polls INT during a HALT or at the end of an instruction. The request will be accepted except when INTE is low or the CPU is in the HOLD condition.
INTE	16	OUT	Interrupts enabled. INTE indicates that an interrupt will be accepted by the TMS 8080 unless it is in the hold state. INTE is set to a high logic level by the EI (Enable Interrupt) instruction and reset to a low logic level by the DI (Disable Interrupt) instruction. INTE is also reset when an interrupt is accepted and by a high on RESET.
DBIN	17	OUT	Data bus in. DBIN indicates whether the data bus is in an input or an output mode. (high = input, low = output).

TABLE 4 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{WR}$	18	OUT	Write. When active (low) $\overline{WR}$ indicates a write operation on the data bus to memory or to an I/O port.
SYNC	19	OUT	Synchronizing control line. When active (high) SYNC indicates the beginning of each machine cycle of the TMS8080. Status information is also present on the data bus during SYNC for external latches.
HLDA	21	OUT	Hold acknowledge. When active (high) HLDA indicates that the TMS8080 is in a hold state.
READY	23	IN	Ready control line. An active (high) level indicates to the TMS 8080 that an external device has completed the transfer of data to or from the data bus. READY is used in conjunction with WAIT for different memory speeds.
WAIT	24	OUT	Wait status. When active (high) WAIT indicates that the TMS8080 has entered a wait state pending a READY signal from memory.

TABLE 5

TMS 8080 STATUS

SIGNATURE	DATA BUS BIT	DESCRIPTION
INTA	D0	Interrupt acknowledge.
$\overline{WO}$	D1	Indicates that current machine cycle will be a read (input) (high = read) or a write (output) (low = write) operation.
STACK	D2	Indicates that address is stack address from the SP.
HLTA	D3	HALT instruction acknowledge.
OUT	D4	Indicates that the address bus has an output device address and the data bus has output data.
M1	D5	Indicates instruction acquisition for first byte.
INP	D6	Indicates address bus has address of input device.
MEMR	D7	Indicates that data bus will be used for memory read data.

2. TMS 8080 INSTRUCTION SET

2.1 INSTRUCTION FORMATS

TMS 8080 instructions are either one, two, or three bytes long and are stored as binary integers in successive memory locations in the format shown below.

One-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE

Two-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D8 D5 D4 D3 D2 D1 D0	OPERAND

Three-Byte Instructions

D7 D6 D5 D4 D3 D2 D1 D0	OP CODE
D7 D6 D5 D4 D3 D2 D1 D0	LOW ADDRESS OR OPERAND 1
D7 D6 D5 D4 D3 D2 D1 D0	HIGH ADDRESS OR OPERAND 2

2.2 INSTRUCTION SET DESCRIPTION

Operations resulting from the execution of TMS 8080 instructions are described in this section. The flags that are affected by each instruction are given after the description.

2.2.1 INSTRUCTION SYMBOLS

SYMBOL	DESCRIPTION
$<b_2>$	Second byte of instruction
$<b_3>$	Third byte of instruction
r_a	Register = / Register Name
	000 / B
	001 / C
	010 / D
	011 / E
	100 / H
	101 / L
	111 / A
r_b	Register = / Register Name
	00 / BC
	01 / DE
	10 / HL
	11 / SP
r_c	Register = / Register Name
	0 / BC
	1 / DE
r_d	Register = / Register Name
	00 / BC
	01 / DE
	10 / HL
r_dL	Least significant 8 bits of r_d
r_dH	Most significant 8 bits of r_d
f	Flags — True condition
	Zero (Z) — Result is zero
	Carry (C) — Carry/borrow out of MSB is one
	Parity (P) — Parity of result is even
	Sign (S) — MSB of result is one
	Carry 1(C1) — Carry out of fourth bit is one
M	Memory address defined by registers H and L
( )	Contents of specified address or register
[ ]	Contents at address contained in specified register
←	Is transferred to
↔	Exchange
Am	Bit m of A register (accumulator)
| |	Flags affected
b_2	Single byte immediate operand
b_3b_2	Double byte immediate operand
$(nnn)_8$	(nnn) is an octal (base 8) number

2.2.2 ACCUMULATOR GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
ACI	b_2	2	2/7	(A) ← (A) + <b_2> + (carry), add the second byte of the instruction and the contents of the carry flag to register A and place in A. |C,Z,S,P,C1|
ADC	M	1	2/7	(A) ← (A) + (M) + (carry). |C,Z,S,P,C1|
ADC	r_a	1	1/4	(A) ← (A) + (r_a) + (carry). |C,Z,S,P,C1|
ADD	M	1	2/7	(A) ← (A) + (M), add the contents of M to register A and place in A. |C,Z,S,P,C1|
ADD	r_a	1	1/4	(A) ← (A) + (r_a). |C,Z,S,P,C1|
ADI	b_2	2	2/7	(A) ← (A) + <b_2>. |C,Z,S,P,C1|
ANA	M	1	2/7	(A) ← (A) AND (M), take the logical AND of M and register A and place in A. The carry flag will be reset low. |C,Z,S,P,C1|
ANA	r_a	1	1/4	(A) ← (A) AND (r_a). |C,Z,S,P,C1|
ANI	b_2	2	2/7	(A) ← (A) AND <b_2>. |C,Z,S,P,C1|
CMA		1	1/4	(A) ← ($\bar{A}$), complement A.
CMC		1	1/4	(carry) ← ($\overline{carry}$), complement the carry flag. |C|
CMP	M	1	2/7	(A) − (M), compare the contents of M to register A and set the flags accordingly. |C,Z,S,P,C1| (A) = (M) Z = 1 (A) ≠ (M) Z = 0 (A) < (M) C = 1 (A) > (M) C = 0
CMP	r_a	1	1/4	(A) − (r_a). |C,Z,S,P,C1|
CPI	b_2	2	2/7	(A)−<b_2>. |C,Z,S,P,C1|
DAA		1	1/4	(A)←BCD correction of (A). The 8 bit A contents is corrected to form two 4 bit BCD digits after a binary arithmetic operation. A fifth flag C1 indicates the overflow from A_3. The carry flag C indicates the overflow from A_7 (See Table 3). |C,Z,S,P,C1|
DAD	r_b	1	1/10	(HL) ← (HL) + (r_b), add the contents of double register r_b to double register HL and place in HL. |C|
LDA	b_3b_2	3	4/13	(A)←[<b_3> <b_2>]
LDAX	r_c	1	2/7	(A)←[(r_c)]
ORA	M	1	2/7	(A) ← (A) OR (M), take the logical OR of the contents of M and register A and place in A. The carry flag will be reset. |C,Z,S,P,C1|
ORA	r_a	1	1/4	(A) ← (A) OR (r_a). |C,Z,S,P,C1|
ORI	b_2	2	2/7	(A) ← (A) OR <b_2>. |C,Z,S,P,C1|
RAL		1	1/4	A_{m+1}←A_m, A_0←(carry), (carry)←(A_7). Shift the contents of register A to the left one bit through the carry flag. |C|
RAR		1	1/4	A_m←A_{m+1}, A_7←(carry), (carry)← A_0. |C|
RLC		1	1/4	A_{m+1}←A_m, A_0←A_7 (carry)←(A_7). Shift the contents of register A to the left one bit. Shift A_7 into A and into the carry flag. |C|
RRC		1	1/4	A_m←A_{m+1}, A_7←A_0, (carry)←(A_0). |C|

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
SBB	M	1	2/7	(A)←(A)−(M)−(carry), subtract the contents of M and the contents of the carry flag from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). |C,Z,S,P,C1|
SBB	r_s	1	1/4	(A)←(A)−(r_s)−(carry). |C,Z,S,P,C1|
SBI	b_2	2	2/7	(A)←(A)−<b_2>−(carry). |C,Z,S,P,C1|
STA	b_3b_2	3	4/13	[<b_3> <b_2>]←(A), store contents of A in memory address given in bytes 2 and 3.
STAX	r_c	1	2/7	[(r_c)]←(A), store contents of A in memory address given in BC or DE.
STC		1	1/4	(carry)←1, set carry flag to a 1 (true condition).
SUB	M	1	2/7	(A)←(A)−(M), subtract the contents of M from register A and place in A. Two's complement subtraction is used and a true borrow causes the carry flag to be set (underflow condition). |C,Z,S,P,C1|
SUB	r_s	1	1/4	(A)←(A)−(r_s).|C,Z,S,P,C1|
SUI	b_2	2	2/7	(A)←(A)−<b_2>. |C,Z,S,P,C1|
XRA	M	1	2/7	(A)←(A) XOR (M), take the exclusive OR of the contents of M and register A and place in A. The carry flag will be reset. |C,Z,S,P,C1|
XRA	r_s	1	1/4	(A)←(A) XOR (r_s). |C,Z,S,P,C1|
XRI	b_2	2	2/7	(A)←(A) XOR <b_2>. |C,Z,S,P,C1|

2.2.3 INPUT/OUTPUT INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
IN	b_2	2	3/10	(A)←(input data from data bus), byte 2 is sent on bits A7-A0 and A15-A8 as the input device address. INP status is given on the data bus.
OUT	b_2	2	3/10	(Output data)←(A), byte 2 is sent on bits A7-A0 and A15-A8 as the output device address. OUT status is given on the data bus.

2.2.4 MACHINE INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
HLT		1	2/7	Halt, all machine operations stop. All registers are maintained. Only an interrupt can return the TMS 8080 to the run mode. Note that a HLT should not be placed in location zero, otherwise after the reset pin is active, the TMS 8080 will enter a nonrecoverable state (until power is removed), i.e., in halt with interrupts disabled. This condition also occurs if a HLT is executed while interrupts are disabled. HLTA status is given on the data bus.
NOP		1	1/4	(PC)←(PC)+1, no operation.

2.2.5 PROGRAM COUNTER AND STACK CONTROL INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
CALL	b_3b_2	3	5/17	[(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PC)←<b_3> <b_2>, transfer PC to the stack address given by SP, decrement SP twice, and jump unconditionally to address given in bytes 2 and 3.
Conditional call instructions for true flags:				
(f)			5/17 (Pass)	If (f) = 1, [(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PS)←<b_3> <b_2>, otherwise (PC)←(PC)+3. If the flag specified, f, is 1, then execute a call. Otherwise, execute the next instruction.
CC (carry)	b_3b_2	3	3/11 (Fail)	
CPE (parity)	b_3b_2	3		
CM (sign)	b_3b_2	3		
CZ (zero)	b_3b_2	3		
Conditional call instructions for false flags:				
(f)			5/17 (Pass)	If (f) = 0, [(SP)−1] [(SP)−2]←(PC), (SP)←(SP)−2, (PC)←<b_3> <b_2>, otherwise (PC)←(PC)+3.
CNC (carry)	b_3b_2	3	3/11 (Fail)	
CPO (parity)	b_3b_2	3		
CP (sign)	b_3b_2	3		
CNZ (zero)	b_3b_2	3		
DI		1	1/4	Disable interrupts. INTE is driven false to indicate that no interrupts will be accepted.
EI		1	1/4	Enable interrupts. INTE is driven true to indicate that an interrupt will be accepted. Execution of this instruction is delayed to allow the next instruction to be executed before the INT input is polled.
JMP	b_3b_2	3	3/10	(PC)←<b_3> <b_2>, jump unconditionally to address given in bytes 2 and 3.
Conditional jump instructions for true flags:				
(f)			3/10	If (f) = 1, (PC)←<b_3><b_2>, otherwise (PC)←(PC)+3. If the flag specified, f, is 1, execute a JMP. Otherwise, execute the next instruction.
JC (carry)	b_3b_2	3		
JPE (parity)	b_3b_2	3		
JM (sign)	b_3b_2	3		
JZ (zero)	b_3b_2	3		
Conditional jump instructions for false flags:				
(f)			3/10	If (f) = 0, (PC)←<b_3> <b_2>, othewise (PC)←(PC)+3.
JNC (carry)	b_3b_2	3		
JPO (parity)	b_3b_2	3		
JM (sign)	b_3b_2	3		
JNZ (zero)	b_3b_2	3		
PCHL		1	1/5	(PC)←(HL)
POP	PSW	1	3/10	(F)←[(SP)], (A)←[(SP)+1], (SP)←(SP)+2, restore the last stack values addressed by SP into A and F. Increment SP twice.
POP	r_d	1	3/10	(r_{dL})←[(SP)], (r_{dH})←[(SP)+1], (SP)←(SP)+2.
PUSH	PSW	1	3/11	[(SP)−1]←(A), [(SP)−2]←(F), (SP)←(SP)−2, save the contents of A and F into the stack addressed by SP. Decrement SP twice.
PUSH	r_d	1	3/11	[(SP)−1]←(r_{dL}), [(SP)−2]←(r_{dH}), (SP)←(SP)−2.
RET		1	3/10	(PC)←[(SP)] [(SP)+1], (SP)←(SP)+2, return to program at memory address given by last values in the stack. The SP is incremented by two.

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
Conditional return instructions for true flags:				
(f)			3/11 (Pass)	If (f) = 1, (PC)←[(SP)] [(SP+1)], (SP)←(SP)+2. If the flag specified, f, is 1, execute a RET. Otherwise, execute the next instruction.
RC (carry)	C	1	1/5 (Fail)	
RPE (parity)	P	1		
RM (sign)	S	1		
RZ (zero)	Z	1		
Conditional return instructions for false flags:				
(f)			3/11 (Pass)	If (f) = 0, (PC)←[(SP)] [(SP)+1], (SP)←(SP)+2.
RNC (carry)	C	1	1/5 (Fail)	
RPO (parity)	P	1		
RP (sign)	S	1		
RNZ (zero)	Z	1		
RST		1	3/11	[(SP)−1] [(SP)−2] ← (PC) (SP)←(SP)−2, (PC)←0000R0_8 where R is a 3 bit field in RST (RST=3R7$_8$). Transfer PC to the stack address given by SP, decrement SP twice, and jump to the address specified by R.
SPHL		1	1/5	(SP)←(HL).

2.2.6 REGISTER GROUP INSTRUCTIONS

MNEMONIC	OPERANDS	BYTES	M CYCLES/ STATES	DESCRIPTION
DCR	M	1	3/10	(M)←(M)−1, decrement the contents of memory location specified by H and L. {Z,S,P,C1}
DCR	r_a	1	1/5	(r_a)←(r_a)−1, decrement the contents of register r_a. {Z,S,P,C1}
DCX	r_b	1	1/5	(r_b)←(r_b)−1, decrement double registers BC, DE, HL, or SP.
INR	M	1	3/10	(M)←(M)+1, increment the contents of memory location specified by H and L. {Z,S,P,C1}
INR	r_a	1	1/5	(r_a)←(r_a)+1, increment the contents of register r_a. {Z,S,P,C1}
INX	r_b	1	1/5	(r_b)←(r_b)+1, increment double registers BC, DE, HL, or SP.
LHLD	b_3b_2	3	5/16	(L)←[<b_3> <b_2>]; (H)←[<b_3> <b_2>+1], load registers H and L with contents of the two memory locations specified by bytes 3 and 2.
LXI	$r_bb_3b_2$	3	3/10	(r_{bH})←<b_3>; (r_{bL})←<b_2>, load double registers BC, DE, HL, or SP immediate with bytes 3, 2, respectively.
MVI	M,b_2	2	3/10	(M)←<b_2>, store immediate byte 2 in the address specified by HL
MVI	r_ab_2	2	2/7	(r_a)←<b_2>, load register r_a immediate with byte 2 of the instruction.
MOV	Mr_a	1	2/7	(M)←(r_a), store register r_a in the memory location addressed by H and L.
MOV	r_aM	1	2/7	(r_a)←(M), load register r_a with contents of memory addressed by HL.
MOV	$r_{a1}r_{a2}$	1	1/5	(r_{a1})←(r_{a2}), load register r_{a1} with contents of r_{a2}. r_{a2} contents remain unchanged.
SHLD	b_3b_2	3	5/16	[<b_3> <b_2>]←(L); [<b_3> <b_2>+1]←(H), store the contents of H and L into two successive memory locations specified by bytes 3 and 2.
XCHG		1	1/4	(H)↔(D); (L)↔(E), exchange double registers HL and DE
XTHL		1	5/18	(L)↔[(SP)], (H)↔[(SP)+1], (SP)=(SP), exchange the top of the stack with register HL.

2.3 INSTRUCTION SET OPCODES ALPHABETICALLY LISTED

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
ACI	2	Add immediate to A with carry†		C	E	7
ADC M	1	Add memory to A with carry†		8	E	7
ADC r	1	Add register to A with carry†	B	8	8	4
			C	8	9	
			D	8	A	
			E	8	B	
			H	8	C	
			L	8	D	
			A	8	F	
ADD M	1	Add memory to A†		8	6	7
ADD r	1	Add register to A†	B	8	0	4
			C	8	1	
			D	8	2	
			E	8	3	
			H	8	4	
			L	8	5	
			A	8	7	
ADI	2	Add immediate to A†		C	6	7
ANA M	1	AND memory with A†		A	6	7
ANAr	1	AND register with A†	B	A	0	4
			C	A	1	
			D	A	2	
			E	A	3	
			H	A	4	
			L	A	5	
			A	A	7	
ANI	2	AND immediate with A†		E	6	7
CALL	3	Call unconditional		C	D	17
CC	3	Call on carry		D	C	11/17
CM	3	Call on minus		F	C	11/17
CMA	1	Complement A		2	F	4
CMC	1	Complement carry‡		3	F	4
CMP M	1	Compare memory with A†		B	E	7
CMP r	1	Compare register with A				
			B	B	8	4
			C	B	9	
			D	B	A	
			E	B	B	
			H	B	C	
			L	B	D	
			A	B	F	
CNC	3	Call on no carry		D	4	11/17
CNZ	3	Call on no zero		C	4	11/17
CP	3	Call on positive		F	4	11/17
CPE	3	Call on parity even		E	C	11/17
CPI	2	Compare immediate with A†		F	E	7
CPO	3	Call on parity odd		E	4	11/17
CZ	3	Call on zero		C	C	11/17
DAA	1	Decimal adjust A†		2	7	4

*Two possible cycle times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES
DAD B	1	Add B&C to H&L‡		0	9	10
DAD D	1	Add D&E to H&L‡		1	9	10
DAD H	1	Add H&L to H&L‡		2	9	10
DAD SP	1	Add stack pointer to H&L‡		3	9	10
DCR M	1	Decrement Memory§		3	5	10
DCR r	1	Decrement Register§	B	0	5	5
			C	0	D	
			D	1	5	
			E	1	D	
			H	2	5	
			L	2	D	
			A	3	D	
DCX B	1	Decrement B&C		0	B	5
DCX D	1	Decrement D&E		1	B	5
DCX H	1	Decrement H&L		2	B	5
DCX SP	1	Decrement stack pointer		3	B	5
DI	1	Disable interrupts		F	3	4
EI	1	Enable interrupts		F	B	4
HLT	1	Halt		7	6	7
IN	2	Input		D	B	10
INR M	1	Increment memory§		3	4	10
INR r	1	Increment register§	B	0	4	5
			C	0	C	
			D	1	4	
			E	1	C	
			H	2	4	
			L	2	C	
			A	3	C	
INX B	1	Increment B&C register		0	3	5
INX D	1	Increment D&E register		1	3	5
INX H	1	Increment H&L register		2	3	5
INX SP	1	Increment stack pointer		3	3	5
JC	3	Jump on carry		D	A	10
JM	3	Jump on minus		F	1	10
JMP	3	Jump unconditional		C	3	10
JNC	3	Jump on no carry		D	2	10
JNZ	3	Jump on no zero		C	2	10
JP	3	Jump on positive		F	2	10
JPE	3	Jump on parity even		E	A	10
JPO	3	Jump on parity odd		E	2	10
JZ	3	Jump on zero		C	A	10
LDA	1	Load A direct		3	A	13
LDAX B	1	Load A indirect		0	A	7
LDAX D	1	Load A indirect		1	A	7
LHLD	3	Load H&L direct		2	A	16
LXI B	3	Load immediate register pair B&C		0	1	10
LXI D	3	Load immediate register pair D&E		1	1	10
LXI H	3	Load immediate register		2	1	10
LXI SP	3	Load immediate stack pointer		3	1	10

‡Only carry flag affected.
§All flags except carry affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES
MOV M,r	1	Move register to memory	B	7	0	7
			C	7	1	
			D	7	2	
			E	7	3	
			H	7	4	
			L	7	5	
			A	7	7	
MOV r,M	1	Move memory to register	B	4	6	7
			C	4	E	
			D	5	6	
			E	5	E	
			H	6	6	
			L	6	E	
			A	7	E	
MOV r_1, r_2	1	Move register to register	B,B	4	0	5
			B,C	4	1	
			B,D	4	2	
			B,E	4	3	
			B,H	4	4	
			B,L	4	5	
			B,A	4	7	
			C,B	4	8	
			C,C	4	9	
			C,D	4	A	
			C,E	4	B	
			C,H	4	C	
			C,L	4	D	
			C,A	4	F	
			D,B	5	0	
			D,C	5	1	
			D,D	5	2	
			D,E	5	3	
			D,H	5	4	
			H,L	5	5	
			D,A	5	7	
			E,B	5	8	
			E,C	5	9	
			E,D	5	A	
			E,E	5	B	
			E,H	5	C	
			E,L	5	D	
			E,A	5	F	
			H,B	6	0	
			H,C	6	1	
			H,D	6	2	
			H,E	6	3	
			H,H	6	4	
			H,L	6	5	
			H,A	6	7	
			L,B	6	8	

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
MOV r1, r2	1	Move register to register (continued)	L,C	6	9	
			L,D	6	A	
			L,E	6	B	
			L,H	6	C	
			L,L	6	D	
			L,A	6	F	
			A,B	7	8	
			A,C	7	9	
			A,D	7	A	
			A,E	7	B	
			A,H	7	C	
			A,L	7	D	
			A,A	7	F	
MVI M	2	Move immediate memory		3	6	10
MVI r	2	Move immediate register	B	0	6	7
			C	0	E	
			D	1	6	
			E	1	E	
			H	2	6	
			L	2	E	
			A	3	E	
NOP	1	No operation	4	0	0	4
ORA M	1	OR memory with A†		B	6	7
ORA r	1	OR register with A†	B	B	0	4
			C	B	1	
			D	B	2	
			E	B	3	
			H	B	4	
			L	B	5	
			A	B	7	
ORI	2	OR immediate with A†		F	6	7
OUT	2	Output		D	3	10
PCHL	1	H&L to program counter		E	9	5
POP B	1	Pop register pair B&C off stack		C	1	10
POP D	1	Pop register pair D&E off stack		D	1	10
POP H	1	Pop register pair H&L off stack		E	1	10
POP PSW	1	Pop A and flags off stack†		F	1	10
PUSH B	1	Push register pair B&C		C	5	11
PUSH D	1	Push register pair D&C		D	5	11
PUSH H	2	Push register pair H&L on stack		E	5	11
PUSH PSW	1	Push A and Flags on stack		F	5	11
RAL	1	Rotate A left through carry		1	7	4
RAR	1	Rotate A right through carry		1	F	4
RC	1	Return on carry		D	8	5/11
RET	1	Return		C	9	10
RLC	1	Rotate A left‡		0	7	4
RM	1	Return on minus		F	8	5/11
RNC	1	Return on no carry		D	0	5/11
RNZ	1	Return on no zero		C	0	5/11
RP	1	Return on positive		F	0	5/11

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, C1) affected.
‡Only carry flag affected.

MNEMONIC	BYTES	DESCRIPTION	REGISTER AFFECTED	POSITIVE-LOGIC HEX OPCODE D7–D4	POSITIVE-LOGIC HEX OPCODE D3–D0	CLOCK CYCLES*
RPE	1	Return on parity even		E	8	5/11
RPO	1	Return on parity odd		E	0	5/11
RRC	1	Rotate A right‡		0	F	4
RST	1	Restart				11
			$PC \leftarrow 0000_{16}$	C	7	
			$PC \leftarrow 0008_{16}$	C	F	
			$PC \leftarrow 0010_{16}$	D	7	
			$PC \leftarrow 0018_{16}$	D	F	
			$PC \leftarrow 0020_{16}$	E	7	
			$PC \leftarrow 0028_{16}$	E	F	
			$PC \leftarrow 0030_{16}$	F	7	
			$PC \leftarrow 0038_{16}$	F	F	
RZ	1	Return on Zero		C	8	5/11
SBB M	1	Subtract memory from A with borrow†		9	E	7
SBB r	1	Subtract register from A with borrow†	B	9	8	4
			C	9	9	
			D	9	A	
			E	9	B	
			H	9	C	
			L	9	D	
			A	9	F	
SBI	2	Subtract immediate from A with borrow†		D	E	7
SHLD	3	Store H&L direct		2	2	16
SPHL	1	H&L to stack pointer		F	9	5
STA	3	Store A direct		3	2	13
STAX B	1	Store A indirect		0	2	7
STAX D	1	Store A indirect		1	2	7
STC	1	Set carry‡		3	7	4
SUB M	1	Subtract memory from A†		9	6	7
SUB r	1	Subtract register from A†	B	9	0	4
			C	9	1	
			D	9	2	
			E	9	3	
			H	9	4	
			L	9	5	
			A	9	7	
SUI	2	Subtract immediate from A†		D	6	7
XCHG	1	Exchange D&E, H&L registers		E	B	4
XRA M	1	Exclusive OR memory with A†		A	E	7
XRA r	1	Exclusive OR register with A†	B	A	8	4
			C	A	9	
			D	A	A	
			E	A	B	
			H	A	C	
			L	A	D	
			A	A	F	
XRI	2	Exclusive OR immediate with A†		E	E	7
XTHL	1	Exchange top of stack H&L		E	3	18

*Two possible cycles times (11/17) indicate instruction cycles dependent on condition flags.
†All flags (C, Z, S, P, CY) affected.
‡Only carry flag affected.

3. TMS 8080 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 20 V
All input and output voltages (see Note 1)	−0.3 V to 20 V
Continuous power dissipation	1.5 W
Operating free-air temperature range	0 C to 70 C
Storage temperature range	−65 C to 150 C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks) (see Note 2)	3.3		$V_{CC}+1$	V
High-level clock input voltage, $V_{IH(\phi)}$	$V_{DD}-1$		$V_{DD}+1$	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 3)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 3)	−1		0.6	V
Operating free-air temperature, T_A	0		70	C

3.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current (any input except clocks and data bus)	V_I = 0 V to V_{CC}			±10	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = 0 V to V_{DD}			±10	μA
$I_{I(DB)}$	Input current, data bus	$V_{I(DB)}$ = 0 V to V_{CC}			−100	μA
$I_{I(hold)}$	Address or data bus input current during hold	$V_{I(ad)}$ or $V_{I(DB)}$ = V_{CC}			10	μA
		$V_{I(ad)}$ or $V_{I(DB)}$ = 0 V			−100	
V_{OH}	High-level output voltage	I_{OH} = 100 μA	3.7			V
V_{OL}	Low-level output voltage	$I_{OL(DB)}$ = 1.7 mA, I_{OL} = 0.75 mA (any output except DB)			0.45	V
$I_{BB(av)}$	Average supply current from V_{BB}	Operating at $t_{c(\phi)}$ = 480 ns, T_A = 25 C		−0.01	−1	mA
$I_{CC(av)}$	Average supply current from V_{CC}			60	75	
$I_{DD(av)}$	Average supply current from V_{DD}			40	67	
C_i	Capacitance, any input except clock	V_{CC} = V_{DD} = V_{SS} = 0 V, V_{BB} = −4.75 to −5.25 V, f = 1 MHz, All other pins at 0 V		10	20	pF
$C_{i(\phi)}$	Clock input capacitance			5	10	
C_o	Output capacitance			10	20	

†All typical values are at T_A = 25 C and nominal voltages

NOTES 2: Active pull up resistors of nominally 2 kΩ will be switched onto the data bus when DBIN is high and the data input voltage is more positive than V_{IH} min.

3: The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

3.4 TIMING REQUIREMENTS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 2)

		MIN	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time (see Note 5)	480	2000	ns
$t_{r(\phi)}$	Clock rise time	5	50	ns
$t_{f(\phi)}$	Clock fall time	5	50	ns
$t_{w(\phi1)}$	Pulse width, clock 1 high	60		ns
$t_{w(\phi2)}$	Pulse width, clock 2 high	220		ns
$t_{d(\phi1L-\phi2)}$	Delay time, clock 1 low to clock 2	0		ns
$t_{d(\phi2-\phi1)}$	Delay time, clock 2 to clock 1	70		ns
$t_{d(\phi1H-\phi2)}$	Delay time, clock 1 high to clock 2 (time between leading edges)	130		ns
$t_{su(da-\phi1)}$	Data setup time with respect to clock 1	50		ns
$t_{su(da-\phi2)}$	Data setup time with respect to clock 2	150		ns
$t_{su(hold)}$	Hold input setup time	140		ns
$t_{su(int)}$	Interrupt input setup time	180		ns
$t_{su(rdy)}$	Ready input setup time	120		ns
$t_{h(da)}$	Data hold time (see Note 6)	$t_{PD(DBI)}$		ns
$t_{h(hold)}$	Hold input hold time	0		ns
$t_{h(int)}$	Interrupt input hold time	0		ns
$t_{h(rdy)}$	Ready input hold time	0		ns

NOTES: 5. $t_{c(\phi)} = t_{d(\phi1L-\phi2)} + t_{r(\phi2)} + t_{w(\phi2)} + t_{f(\phi2)} + t_{d(\phi2-\phi1)} + t_{r(\phi1)}$ 480 ns $\leq t_{c(\phi)} \leq$ 2000 ns.
6. The data input should be enabled using the DBIN status signal. No bus conflict can then occur and the data hold time requirement is thus assured

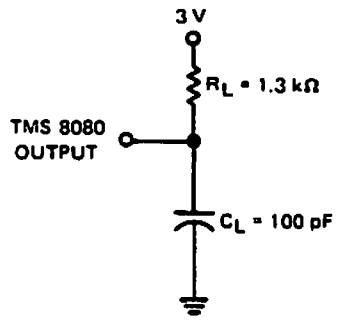
3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURE 2)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{PD(ad)}$	Propagation delay time, clock 2 to address outputs	C_L = 100 pF, R_L = 1.3 kΩ		200	ns
$t_{PD(da)}$	Propagation delay time, clock 2 to data bus			220	ns
$t_{PD(cont)}$	Propagation delay time, clocks to control outputs			120	ns
$t_{PD(DBI)}$	Propagation delay time, clock 2 to DBIN output		25	140	ns
$t_{PD(int)}$	Propagation delay time, clock 2 to INTE output			200	ns
t_{DI}	Time for data bus to enter input mode			$t_{PD(DBI)}$	ns
t_{PXZ}	Disable time to high-impedance state during hold (address outputs and data bus)			120	ns

The time that the address outputs and output data will remain stable after $\overline{WR}$ goes high, t_{WA} and $t_{WD} \geq t_{d(\phi1H-\phi2)}$.
The time between address outputs becoming stable and $\overline{WR}$ going low, $t_{AW} \leq 2\,t_{c(\phi)} - t_{d(\phi1H-\phi2)} - t_{r(\phi)} - 120$ ns.
The time between output data becoming stable and $\overline{WR}$ going low, $t_{DW} \geq t_{c(\phi)} - t_{d(\phi1H-\phi2)} - t_{r(\phi)} - 150$ ns.
The following are relevant when interfacing to devices requiring V_{IH} min of 3.3 V:

a) Maximum output rise time (t_{TLH}) from 0.8 V to 3.3 V is 140 ns with C_L as specified for the propagation delay times above.

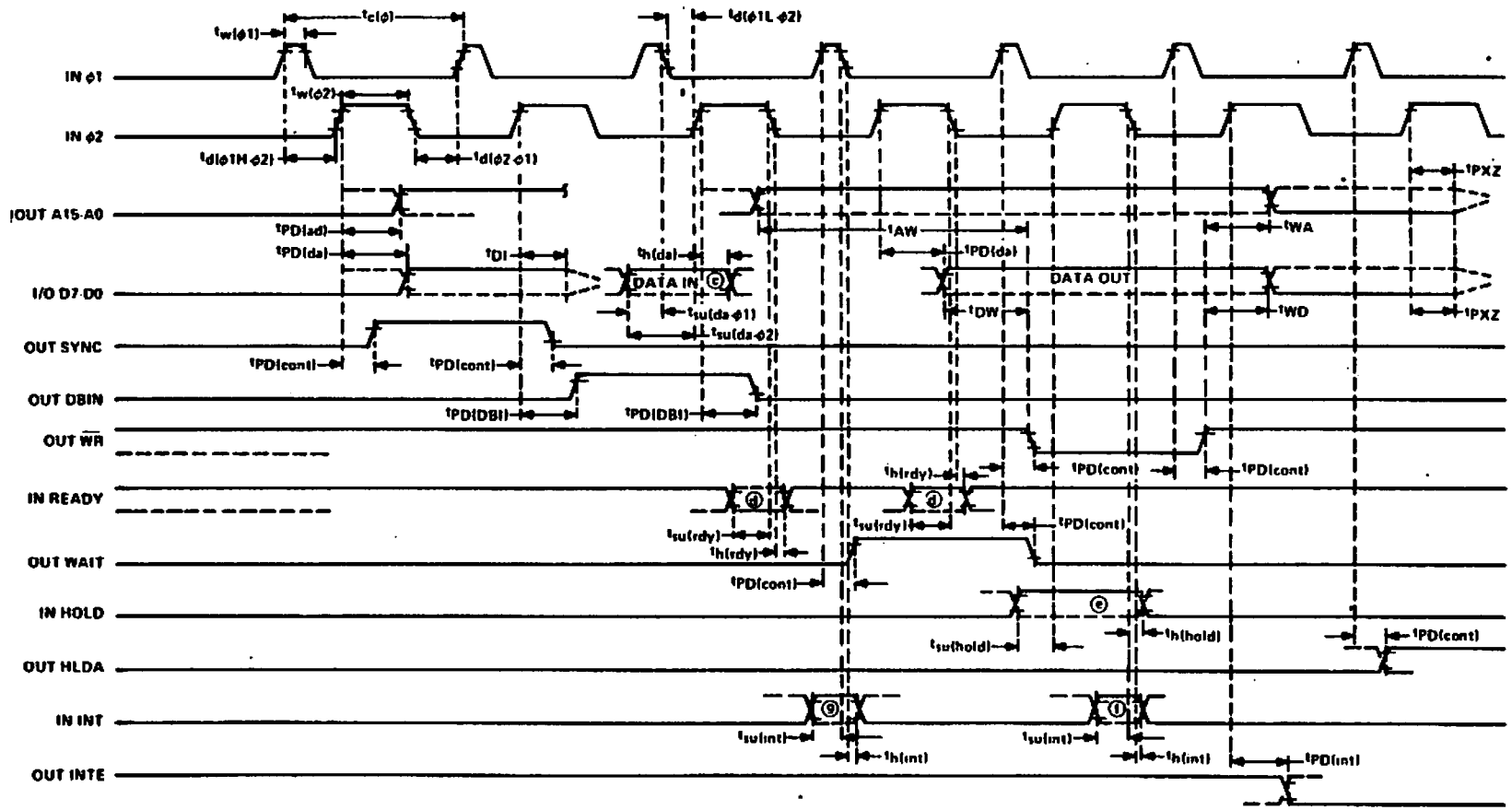
b) Maximum propagation delay times when measured to $V_{ref(H)}$ = 3 V (instead of 2 V) will be 60 ns more than as specified above with C_L as specified.



C_L includes probe and jig capacitance.

LOAD CIRCUIT

voltage waveforms (see notes a and b)

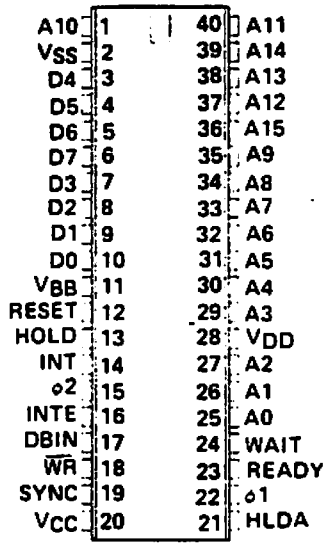


NOTES:
a. This timing diagram shows timing relationships only, it does not represent any specific machine cycle.
b. Time measurements are made at the following reference voltages: Clock, $V_{ref(H)}$ = 9.5 V, $V_{ref(L)}$ = 1 V. Other inputs, $V_{ref(H)}$ = 2 V, $V_{ref(L)}$ = 0.8 V.
c. Data in must be stable for this period when DBIN is high during S3. Requirements for both $t_{su(da\,\phi1)}$ and $t_{su(da\,\phi2)}$ must be satisfied.
d. The ready signal must be stable for this period during S2 or SW. This requires external synchronization.
e. The hold signal must be stable for this period during S2 or SW when entering the hold mode and during S3, S4, S5 and SWH when in the hold mode. This requires external synchronization.
f. The interrupt signal must be stable during this period on the last clock cycle of any instruction to be recognized on the following instruction. External synchronization is not required.
g. During halt mode only, timing is with respect to the clock 1 falling edge.

FIGURE 2

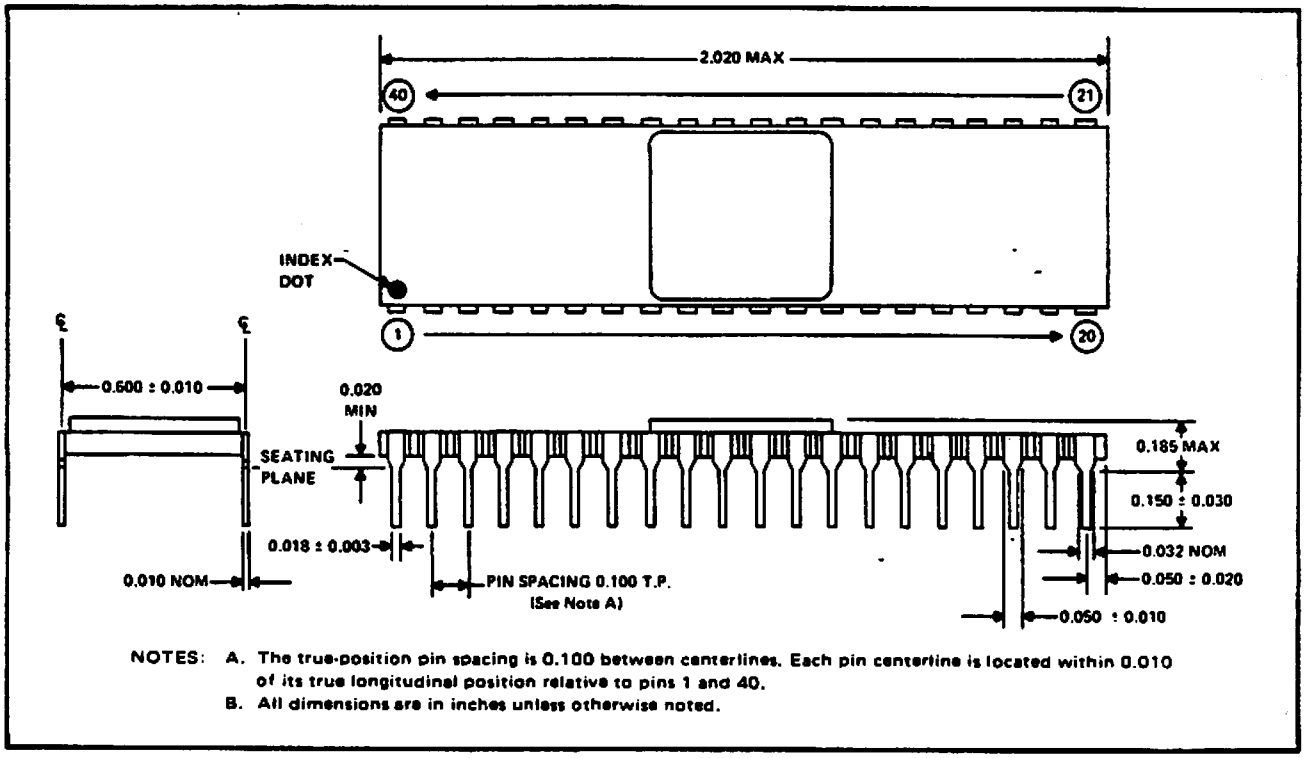
3.6 TERMINAL ASSIGNMENTS

TMS 8080



3.7 MECHANICAL DATA

40-PIN CERAMIC PACKAGE



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within 0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches unless otherwise noted.

Appendix B

TMS 5501 Multifunction Input/Output Controller

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TMS 5501 MULTIFUNCTION INPUT/OUTPUT CONTROLLER

1. INTRODUCTION

1.1 DESCRIPTION

The TMS 5501 is a multifunction input/output circuit for use with TI's TMS 8080 CPU. It is fabricated with the same N-channel silicon-gate process as the TMS 8080 and has compatible timing, signal levels, and power supply requirements. The TMS 5501 provides a TMS 8080 microprocessor system with an asynchronous communications interface, data I/O buffers, interrupt control logic, and interval timers.

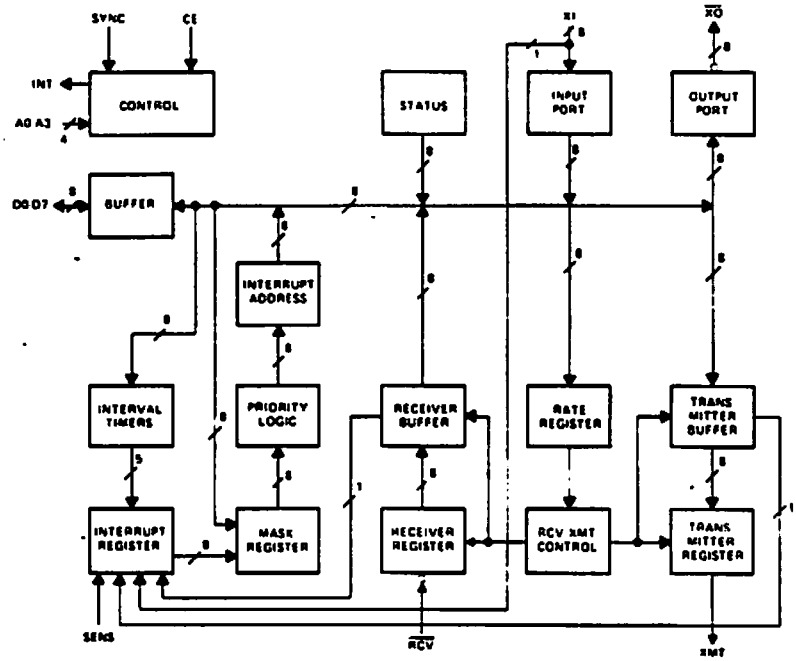


FIGURE 1–TMS 5501 BLOCK DIAGRAM

The I/O section of the TMS 5501 contains an eight-bit parallel input port and a separate eight-bit parallel output port with storage register. Five programmable interval timers provide time intervals from 64 μs to 16.32 ms.

The interrupt system allows the processor to effectively communicate with the interval timers, external signals, and the communications interface by providing TMS 8080-compatible interrupt logic with masking capability.

Data transfers between the TMS 5501 and the CPU are carried by the data bus and controlled by the interrupt, chip enable, sync, and address lines. The TMS 8080 uses four of its memory-address lines to select one of 14 commands to which the TMS 5501 will respond. These commands allow the CPU to:

- read the receiver buffer
- read the input port
- read the interrupt address
- read TMS 5501 status
- issue discrete commands
- load baud rate register
- load the transmitter buffer
- load the output port
- load the mask register
- load an interval timer

The commands are generated by executing memory referencing instructions such as MOV (register to memory) with the memory address being the TMS 5501 command. This provides a high degree of flexibility for I/O operations by letting the systems programmer use a variety of instructions.

1.2 SUMMARY OF OPERATION

Addressing the TMS 5501

A convenient method for addressing the TMS 5501 is to tie the chip enable input to the highest order address line of the CPU's 16-bit address bus and the four TMS 5501 address inputs to the four lowest order bits of the bus. This, of course, limits the system to 32,768 words of memory but in many applications the full 65,536 word memory addressing capability of the TMS 8080 is not required.

Communications Functions

The communications section of the TMS 5501 is an asynchronous transmitter and receiver for serial communications and provides the following functions:

Programmable baud rate – A CPU command selects a baud rate of 110, 150, 300, 1200, 2400, 4800, or 9600 baud.

Incoming character detection – The receiver detects the start and stop bits of an incoming character and places the character in the receive buffer.

Character transmission – The transmitter generates start and stop bits for a character received from the CPU and shifts it out.

Status and command signals – Via the data bus, the TMS 5501 signals the status of: framing error and overrun error flags; data in the receiver and transmitter buffers; start and data bit detectors; and end-of-transmission (break) signals from external equipment. It also issues break signals to external equipment.

Data Interface

The TMS 5501 moves data between the CPU and external devices through its internal data bus, input port, and output port. When data is present on the bus that is to be sent to an external device, a Load Output Port (LOP) command from the CPU puts the data on the $\overline{XO}$ pins of the TMS 5501 by latching it in the output port. The data remains in the port until another LOP command is received. When the CPU requires data that is present on the External Input (XI) lines, it issues a command that gates the data onto the internal data bus of the TMS 5501 and consequently onto the CPU's data bus at the correct time during the CPU cycles.

Interval Timers

To start a countdown by any of the five interval timers, the program selects the particular timer by an address to the TMS 5501 and loads the required interval into the timer via the data bus. Loading the timer activates it and it counts down in increments of 64 microseconds. The 8-bit counters provide intervals that vary in duration from 64 to 16,320 microseconds. Much longer intervals can be generated by cascading the timers through software. When a timer reaches zero, it generates an interrupt that typically will be used to point to a subroutine that performs a servicing function such as polling a peripheral or scanning a keyboard. Loading an interval value of zero causes an immediate interrupt. A new value loaded while the interval timer is counting overrides the previous value and the interval timer starts counting down the new interval. When an interval timer reaches zero it remains inactive until a new interval is loaded.

Servicing Interrupts

The TMS 5501 provides a TMS 8080 system with several interrupt control functions by receiving external interrupt signals, generating interrupt signals, masking out undersired interrupts, establishing the priority of interrupts, and generating RST instructions for the TMS 8080. An external interrupt is received on pin 22, SENS. An additional external interrupt can be received on pin 32, XI7, if selected by a discrete command from the TMS 8080 (See Figure 4). The TMS 5501 generates an interrupt when any of the five interval timers count to zero. Interrupts are also generated when the receiver buffer is loaded and when the transmitter buffer is empty.

When an interrupt signal is received by the interrupt register from a particular source, a corresponding bit is set and gated to the mask register. A pattern will have previously been set in the mask register by a load-mask-register command from the TMS 8080. This pattern determines which interrupts will pass through to the priority logic. The priority logic allows an interrupt to generate an RST instruction to the TMS 8080 only if there is no higher priority interrupt that has not been accepted by the TMS 8080. The TMS 5501 prioritizes interrupts in the order shown below:

1st – Interval Timer #1
2nd – Interval Timer #2
3rd – External Sensor
4th – Interval Timer #3
5th – Receiver Buffer Loaded
6th – Transmitter Buffer Emptied
7th – Interval Timer #4
8th – Interval Timer #5 or an External Input (XI 7)

The highest priority interrupt passes through to the interrupt address logic, which generates the RST instruction to be read by the TMS 8080. See Table 3 for relationship of interrupt sources to RST instructions and Figures 6 and 8 for timing relationships.

The TMS 5501 provides two methods of servicing interrupts; an interrupt-driven system or a polled-interrupt system. In an interrupt-driven system, the INT signal of the TMS 5501 is tied to the INT input of the TMS 8080. The sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt signal and readies the appropriate RST instruction. (2) The TMS 5501 INT output, tied to the TMS 8080 INT input, goes high signaling the TMS 8080 that an interrupt has occured. (3) If the TMS 8080 is enabled to accept interrupts, it sets the INTA (interrupt acknowledge) status bit high at SYNC time of the next machine cycle. (4) If the TMS 5501 has previously received an interrupt-acknowledge-enable command from the CPU (see Bit 3, Paragraph 2.2.5), the RST instruction is transferred to the data bus.

In a polled-interrupt system, INT is not used and the sequence of events will be: (1) The TMS 5501 receives (or generates) an interrupt and readies the RST instruction. (2) The TMS 5501 interrupt-pending status bit (see Bit 5, Paragraph 2.2.4) is set high (the interrupt-pending status bit and the INT output go high simultaneously). (3) At the prescribed time, the TMS 8080 polls the TMS 5501 to see if an interrupt has occurred by issuing a read-TMS 5501-status command and reading the interrupt-pending bit. (4) If the bit is high, the TMS 8080 will then issue a read-interrupt-address command, which causes the TMS 5501 to transfer the RST instruction to the data bus as data for the instruction being executed by the TMS 8080.

1.3 APPLICATIONS

Communications Terminals

The functions of the TMS 5501 make it particularly useful in TMS 8080-based communications terminals and generally applicable in systems requiring periodic or random servicing of interrupts, generation of control signals to external devices, buffering of data, and transmission and reception of asynchronous serial data. As an example, a system configuration such as shown in Figure 2 can function as the controller for a terminal that governs employee entrance into a plant or security areas within a plant. Each terminal is identified by a central computer through ID switches. The central system supplies each terminal's RAM with up to 16 employee access categories applicable to that terminal. These categories are compared with an employee's badge character when he inserts his badge into the badge sensor. If a

match is not found, a reject light will be activated. If a match is found, the terminal will transmit the employee's badge number and access category to the central system, and a door unlock solenoid will be activated for 4 seconds. The central computer then may take the transmitted information and record it along with time and date of access.

The TMS 4700 is a 1024 x 8 ROM that contains the system program, and the TMS 4036 is a 64 x 8 RAM that serves as the stack for the TMS 8080 and storage for the access category information. TTL circuits control chip-enable information carried by the address bus. Signals from the CPU gate the address bits from the ROM, the RAM, or the TMS 5501 onto the data bus at the correct time in the CPU cycle. The clock generator consists of four TTL circuits along with a crystal, needed to maintain accurate serial data assembly and disassembly with the central computer.

The TMS 5501 handles the asynchronous serial communication between the TMS 8080 and the central system and gates data from the badge reader onto the data bus. It also gates control and status data from the TMS 8080 to the door lock and badge reader and controls the time that the door lock remains open. The TMS 5501 signals the TMS 8080 when the badge reader or the communication lines need service. The functions that the TMS 5501 is to perform are selected by an address from the TMS 8080 with the highest order address line tied to the TMS 5501 chip enable input and the four lowest order lines tied to the address inputs.

2. OPERATIONAL AND FUNCTIONAL DESCRIPTION

This detailed description of the TMS 5501 consists of:

INTERFACE SIGNALS – a definition of each of the circuit's external connections

COMMANDS – the address required to select each of the TMS 5501 commands and a description of the response to the command.

2.1 INTERFACE SIGNALS

The TMS 5501 communicates with the TMS 8080 via four address lines: a chip enable line, an eight-bit bidirectional data bus, an interrupt line, and a sync line. It communicates with system components other than the CPU via eight external inputs, eight external outputs, a serial receiver input, a serial transmitter output, and an external sensor input. Table 1 defines the TMS 5501 pin assignments and describes the function of each pin.

TABLE 1
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
CE	18	Chip enable–When CE is low, the TMS 5501 address decoding is inhibited, which prevents execution of any of the TMS 5501 commands.
A3	17	Address bus–A3 through A0 are the lines that are addressed by the TMS 8080 to select a particular
A2	16	TMS 5501 function.
A1	15	
A0	14	
SYNC	19	Synchronizing signal–The SYNC signal is issued by the TMS 8080 and indicates the beginning of a machine cycle and availability of machine status. When the SYNC signal is active (high), the TMS 5501 will monitor the data bus bits D0 (interrupt acknowledge) and D1 ($\overline{WO}$, data output function).
$\overline{RCV}$	5	Receiver serial data input line–$\overline{RCV}$ must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receive circuitry.

TABLE 1 (continued)
TMS 5501 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	DESCRIPTION
		INPUTS
XI 0	39	External inputs—These eight external inputs are gated to the data bus when the read-external-inputs function is addressed. External input n is gated to data bus bit n without conversion.
XI 1	38	
XI 2	37	
XI 3	36	
XI 4	35	
XI 5	34	
XI 6	33	
XI 7	32	
SENS	22	External interrupt sensing – A transition from low to high at SENS sets a bit in the interrupt register, which, if enabled, generates an interrupt to the TMS 8080.
		OUTPUTS
$\overline{XO}$ 0	24	External outputs—These eight external outputs are driven by the complement of the output register; i.e., if output register bit n is loaded with a high (low) from data bus bit n by a load-output register command, the external output n will be a low (high). The external outputs change only when a load-output-register function is addressed.
$\overline{XO}$ 1	25	
$\overline{XO}$ 2	26	
$\overline{XO}$ 3	27	
$\overline{XO}$ 4	28	
$\overline{XO}$ 5	29	
$\overline{XO}$ 6	30	
$\overline{XO}$ 7	31	
XMT	40	Transmitter serial data output line—This line remains high when the TMS 5501 is not transmitting.
		DATA BUS INPUT/OUTPUT
D0	13	Data bus – Data transfers between the TMS 5501 and the TMS 8080 are made via the 8-bit bidirectional data bus. D0 is the LSB. D7 is the MSB.
D1	12	
D2	11	
D3	10	
D4	9	
D5	8	
D6	7	
D7	6	
INT	23	Interrupt—When active (high), the INT output indicates that at least one of the interrupt conditions has occurred and that its corresponding mask-register bit is set.
		POWER AND CLOCKS
V_{SS}	4	Ground reference
V_{BB}	1	Supply voltage (–5 V nominal)
V_{CC}	2	Supply voltage (5 V nominal)
V_{DD}	3	Supply voltage (12 V nominal)
$\phi 1$	20	Phase 1 clock
$\phi 2$	21	Phase 2 clock

2.2 TMS 5501 COMMANDS

The TMS 5501 operates as input/output device for the TMS 8080. Functions are initiated via the TMS 8080 address bus and the TMS 5501 address inputs. Address decoding to determine the command function being issued is defined in Table 2.

TABLE 2
COMMAND ADDRESS DECODING
When Chip Enable Is High

#2 5501 PORT NO.	#1 5501 PORT NO.	A3	A2	A1	A0	COMMAND	FUNCTION	PARAGRAPH
16	0	L	L	L	L	Read receiver buffer	RBn → Dn	2.2.1
17	1	L	L	L	H	Read external inputs	XIn → Dn	2.2.2
18	2	L	L	H	L	Read interrupt address	RST → Dn	2.2.3
19	3	L	L	H	H	Read TMS 5501 status	(Status) → Dn	2.2.4
20	4	L	H	L	L	Issue discrete commands	See Fig.4	2.2.5
21	5	L	H	L	H	Load rate register	See Fig.4	2.2.6
22	6	L	H	H	L	Load transmitter buffer	Dn → TBn	2.2.7*
23	7	L	H	H	H	Load Output port	Dn → XOn	2.2.8
24	8	H	L	L	L	Load mask register	Dn → MRn	2.2.9
25	9	H	L	L	H	Load interval timer 1	Dn → Timer 1	2.2.10
26	10	H	L	H	L	Load interval timer 2	Dn → Timer 2	2.2.10
27	11	H	L	H	H	Load interval timer 3	Dn → Timer 3	2.2.10
28	12	H	H	L	L	Load interval timer 4	Dn → Timer 4	2.2.10
29	13	H	H	L	H	Load interval timer 5	Dn → Timer 5	2.2.10
30	14	H	H	H	L	No function		
31	15	H	H	H	H	No function		

* Important

RBn Receiver buffer bit n
Dn Data bus I/O terminal n
XIn External input terminal n
RST 11 ($1A_5$) ($1A_4$) ($1A_3$) 1 1 1 (see Table 3)
TBn Transmit buffer bit n
XOn Output register bit n
MRn Mask register bit n

TABLE 3
RST INSTRUCTIONS

DATA BUS BIT 0	1	2	3	4	5	6	7	INTERRUPT CAUSED BY	#1 TMS 5501
H	H	H	L	L	L	H	H	Interval Timer 1	Power Up
H	H	H	H	L	L	H	H	Interval Timer 2	User Timer
H	H	H	L	H	L	H	H	External Sensor	Keyboard
H	H	H	H	H	L	H	H	Interval Timer 3	Repeat Key
H	H	H	L	L	H	H	H	Receiver Buffer	Rx RS-232
H	H	H	H	L	H	H	H	Transmitter Buffer	Tx RS-232
H	H	H	L	H	H	H	H	Interval Timer 4	Bell Timer
H	H	H	H	H	H	H	H	Interval Timer 5 of X17	CRT Executive Loop

The following paragraphs define the functions of the TMS 5501 commands.

2.2.1 Read receiver buffer

Addressing the read-receiver-buffer function causes the receiver buffer contents to be transferred to the TMS 8080 and clears the receiver-buffer-loaded flag.

2.2.2 Read external input lines

Addressing the read-external-inputs function transfers the states of the eight external input lines to the TMS 8080.

2.2.3 Read interrupt address

Addressing the read interrupt address function transfers the current highest priority interrupt address onto the data bus as read data. After the read operation is completed, the corresponding bit in the interrupt register is reset.

If the read-interrupt-address function is addressed when there is no interrupt pending, a false interrupt address will be read. TMS 5501 status function should be addressed in order to determine whether or not an interrupt condition is pending.

2.2.4 Read TMS 5501 status

Addressing the read-TMS 5501-status function gates the various status conditions of the TMS 5501 onto the data bus. The status conditions, available as indicated in Figure 3, are described in the following paragraphs.

BIT:	7	6	5	4	3	2	1	0
	START BIT DETECT	FULL BIT DETECT	INTRPT PENDING	XMIT BUFFER EMPTY	RCV BUFFER LOADED	SERIAL RCVD	OVERRUN ERROR	FRAME ERROR

FIGURE 3–DATA BUS ASSIGNMENTS FOR TMS 5501 STATUS

Bit 0, framing error

A high in bit 0 indicates that a framing error was detected on the last character received (either one or both stop bits were in error). The framing error flag is updated at the end of each character. Bit 0 of the TMS 5501 status will remain high until the next valid character is received.

Bit 1, overrun error

A high in bit 1 indicates that a new character was loaded into the receiver buffer before a previous character was read out. The overrun error flag is cleared each time the read-I/O-status function is addressed or a reset command is issued.

Bit 2, serial received data

Bit 2 monitors the receiver serial data input line. This line is provided as a status input for use in detecting a break and for test purposes. Bit 2 is normally high when no data is being received.

Bit 3, receiver buffer loaded

A high in bit 3 indiciates that the receiver buffer is loaded with a new character. The receiver-buffer-loaded flag remains high until the read-receiver-buffer function is addressed (at which time the flag is cleared). The reset function also clears this flag.

Bit 4, transmitter buffer empty
A high in bit 4 indicates that the transmitter buffer register is empty and ready to accept a character. Note, however, that the serial transmitter register may be in the process of shifting out a character. The reset function sets the transmitter-buffer-empty flag high.

Bit 5, interrupt pending
A high in bit 5 indicates that one or more of the interrupt conditions has occured and the corresponding interrupt is enabled. This bit is the status of the interrupt signal INT.

Bit 6, full bit detected
A high in bit 6 indicates that the first data bit of a receive-data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

Bit 7, start bit detected
A high in bit 7 indicates that the start bit of an incoming data character has been detected. This bit remains high until the entire character has been received or until a reset is issued and is provided for test purposes.

2.2.5 Issue discrete commands

Addressing the discrete command function causes the TMS 5501 to interpret the data bus information according to the following descriptions. See Figure 4 for the discrete command format. Bits 1 through 5 are latched until a different discrete command is received.

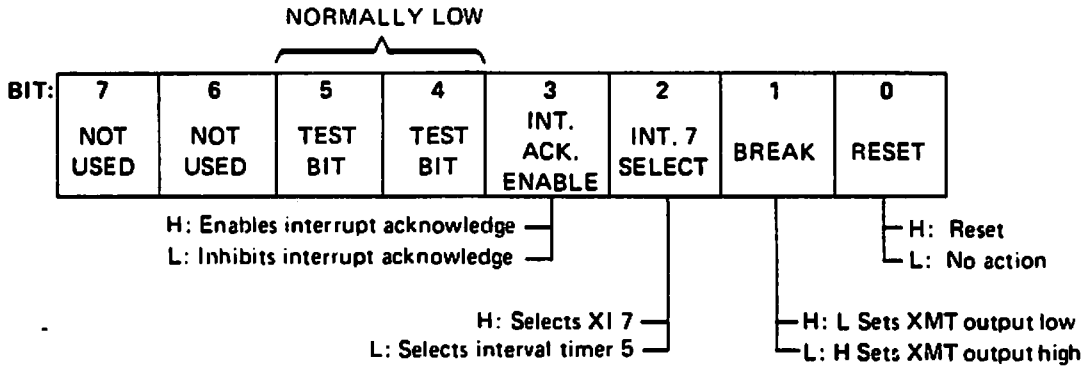


FIGURE 4–DISCRETE COMMAND FORMAT

Bit 0, reset
A high in bit 0 will cause the following:

1) The receiver buffer and register are cleared to the search mode including the receiver-buffer-loaded flag, the start-bit-detected flag, the full-bit-detected flag, and the overrun-error flag. The receiver buffer is not cleared and will contain the last character received.
2) The transmitter data output is set high (marking). The transmitter-buffer-empty flag is set high indicating that the transmitter buffer is ready to accept a character from the TMS 8080.
3) The interrupt register is cleared except for the bit corresponding to the transmitter buffer interrupt, which is set high.
4) The interval timers are inhibited.

A low in bit 0 causes no action. The reset function has no affect on the output port, the external inputs, interrupt acknowledge enable, the mask register, the rate register, the transmitter register, or the transmitter buffer.

Bit 1, break
A low in bit 1 causes the transmitter data output to be reset low (spacing).

If bit 0 and bit 1 are both high, the reset function will override.

Bit 2, interrupt 7 select
Interrupt 7 may be generated either by a low to high transition of external input 7 or by interval timer 5.

A high in bit 2 selects the interrupt 7 source to be the transition of external input 7. A low in bit 2 selects the interrupt 7 source to be interval timer 5.

Bit 3, interrupt acknowledge enable
The TMS 5501 decodes data bus (CPU status) bit 0 at SYNC of each machine cycle to determine if an interrupt acknowledge is being issued.

A high in bit 3 enables the TMS 5501 to accept the interrupt acknowledge decode. A low in bit 3 causes the TMS 5501 to ignore the interrupt acknowledge decode.

Bit 4 and bit 5 are used only during testing of the TMS 5501. For correct system operation both bits must be kept low.

Bit 6 and bit 7 are not used and can assume any value.

2.2.6 Load rate register

Addressing the load-rate-register function causes the TMS 5501 to load the rate register from the data bus and interpret the data bits (See Figure 5) as follows.

BIT:	7	6	5	4	3	2	1	0
	STOP BIT(s)	9600 baud	4800 baud	2400 baud	1200 baud	300 baud	150 baud	110 baud

H: One stop bit
L: Two stop bits

FIGURE 5–DATA BUS ASSIGNMENTS FOR RATE COMMANDS

Bits 0 through 6, rate select

The rate select bits (bits 0 through 6) are mutually exclusive, i.e., only one bit may be high. A high in bits 0 through 6 will select the baud rate for both the transmitter and receiver circuitry as defined below and in Figure 5:

Bit 0 110 baud
Bit 1 150 baud
Bit 2 300 baud
Bit 3 1200 baud
Bit 4 2400 baud
Bit 5 4800 baud
Bit 6 9600 baud

If more than one bit is high, the highest rate indicated will result. If bits 0 through 6 are all low, both the receiver and the transmitter circuitry will be inhibited.

Bit 7, stop bits

Bit 7 determines whether one or two stop bits are to be used by both the transmitter and receiver circuitry. A high in bit 7 selects one stop bit. A low in bit 7 selects two stop bits.

2.2.7 Load transmitter buffer

Addressing the load-transmitter-buffer function transfers the state of the data bus into the transmitter buffer.

2.2.8 Load output port

Addressing the load-output-port function transfers the state of the data bus into the output port. The data is latched and remains on $\overline{XO}$ 0 through $\overline{XO}$ 7 as the complement of the data bus until new data is loaded.

2.2.9 Load mask register

Addressing the load-mask-register function loads the contents of the data bus into the mask register. A high in data bus bit n enables interrupt n. A low inhibits the corresponding interrupt.

2.2.10 Load timer n

Addressing the load-timer-n function loads the contents of the data bus into the appropriate interval timer. Time intervals of from 64 μs (data bus = LLLLLLLH) to 16,320 μs (data bus HHHHHHHH) are counted in 64-μs, steps. When the count of interval timer n reaches 0, the bit in the interrupt register that corresponds to timer n is set and an interrupt is generated. Loading all lows causes an interrupt immediately.

3. TMS 5501 ELECTRICAL AND MECHANICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{DD} (see Note 1	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 20 V
All input and output voltages (see Note 1)	−0.3 V to 20 V
Continuous power dissipation	1.1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the normally most negative supply voltage, V_{BB} (substrate). Throughout the remainder of this data sheet, voltage values are with respect to V_{SS} unless otherwise noted.

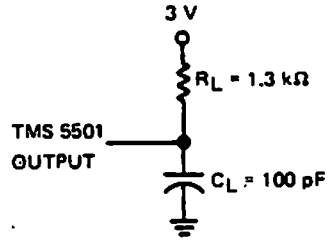
3.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (all inputs except clocks)	3.3		V_{CC}+1	V
High-level clock input voltage, $V_{IH(\phi)}$	V_{DD}−1		V_{DD}+1	V
Low-level input voltage, V_{IL} (all inputs except clocks) (see Note 2)	−1		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$ (see Note 2)	−1		0.6	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this specification for logic voltage levels only.

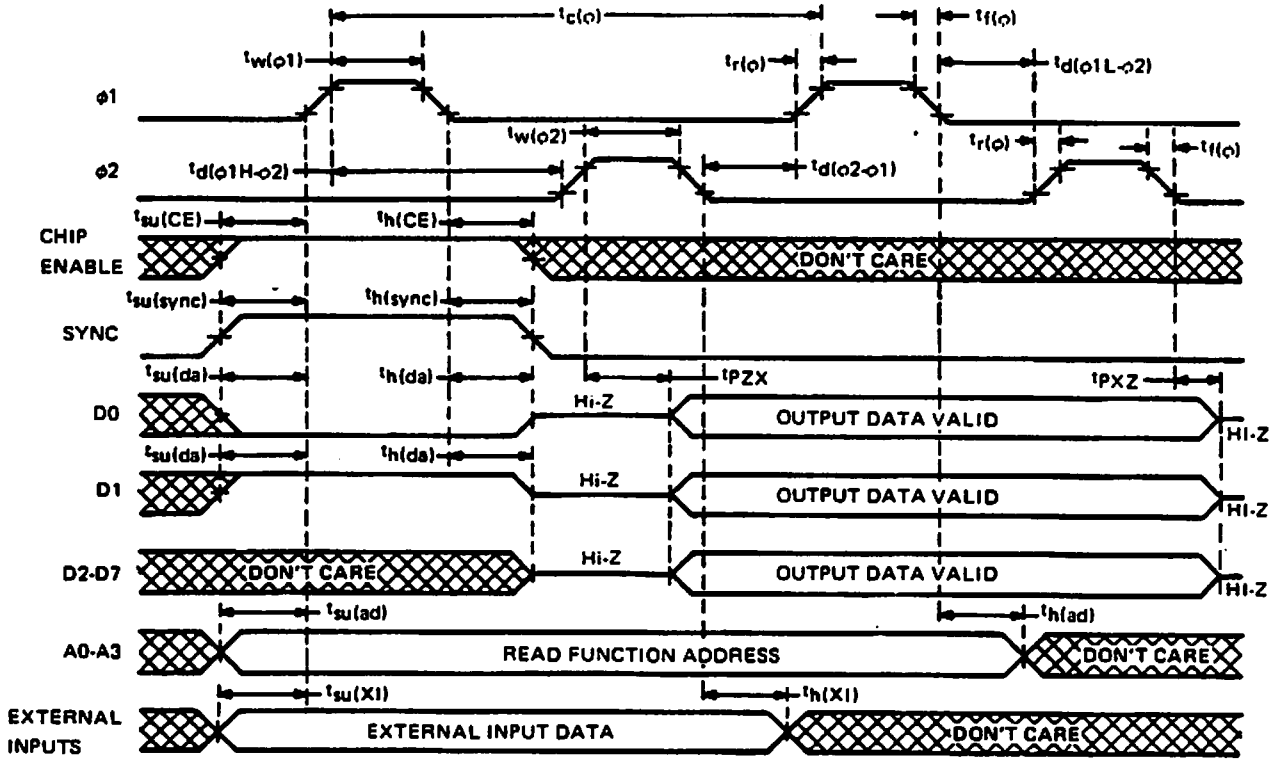
3.5 SWITCHING CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS (SEE FIGURES 6 AND 7)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PZX}	Data bus output enable time	C_L = 100 pF, R_L = 1.3 kΩ		200*	ns
t_{PXZ}	Data bus output disable time to high-impedance state			180	ns
t_{PD}	External data output propagation delay time from ϕ2			200	ns



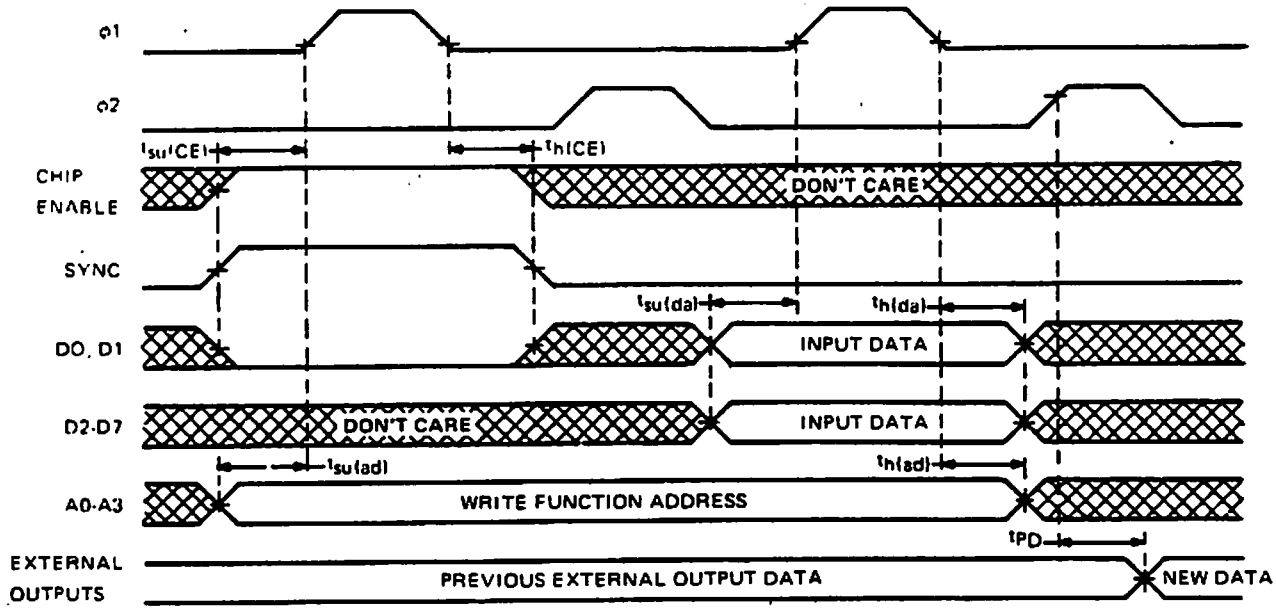
C_L includes probe and jig capacitance

LOAD CIRCUIT



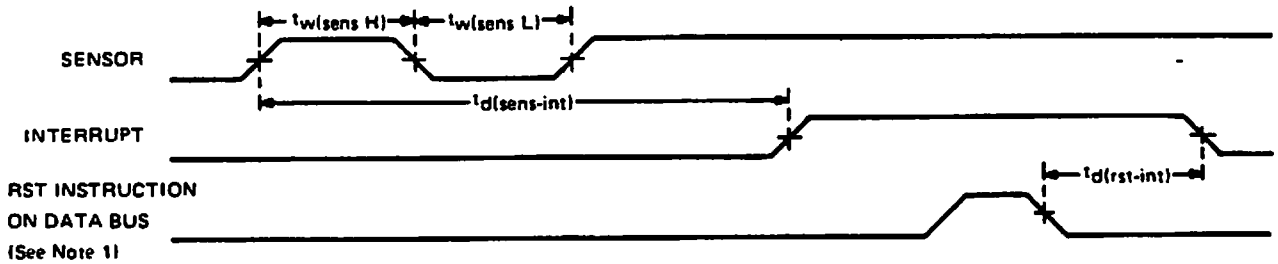
NOTE: For ϕ1 or ϕ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 6–READ CYCLE TIMING



NOTE: For φ1 and φ2 inputs, high and low timing points are 90% and 10% of $V_{IH(\phi)}$. All other timing points are the 50% level.

FIGURE 7—WRITE CYCLE TIMING



NOTES: 1 The RST instruction occurs during the output data valid time of the read cycle.
2 All timing points are 50% of V_{IH}.

FIGURE 8—SENSOR/INTERRUPT TIMING

The 5048 CRT Controller is similar to the 5027. It differs in that pin 10 is used for 50/60 Hz. Sync input rather than for composite sync output. The 5048-003 is masked for the 64 x 32 format as used by the 3600 Series Intecolor units; thus loading of some registers at power-up is not required. (The 5048-004 is masked for the 80 x 48 format.)

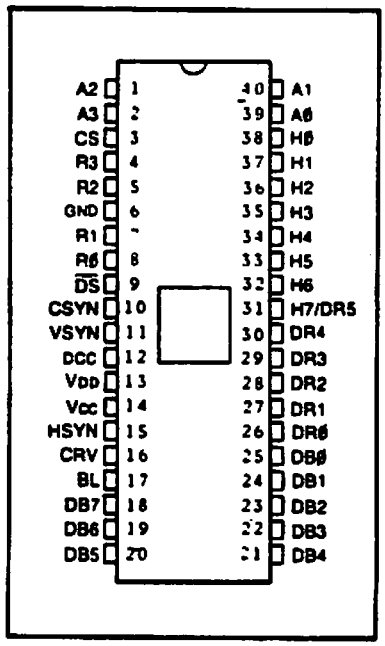
CRT 5027
Preliminary Product Description

CRT Video Timer-Controller VTAC

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row
  - Data rows per frame
  - Raster scans per data row
  - Raster scans per frame
- ☐ Fully Programmable Monitor Format
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Scrolling
- ☐ Generation of Cursor Video
- ☐ Interlaced and Non-interlaced Operation
- ☐ Vertical Data Positioning
- ☐ TTL Compatibility
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology

PIN CONFIGURATION



General Description

The CRT Video Timer-Controller Chip (VTAC) is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to + 150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+18.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V±5%, V_{DD}= +12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	Vcc−1.5		Vcc	V	
OUTPUT VOLTAGE LEVELS					
Low Level—V_{OL} for RØ-3			0.4	V	I_{OL} = 3.2ma
Low Level—V_{OL} all others			0.4	V	I_{OL} = 1.6ma
High Level—V_{OH} for RØ-3	2.4				I_{OH} = 80μa
High Level—V_{OH} all others	2.4				I_{OH} = 40μa
INPUT CURRENT					
Low Level, I_{IL}					
High Level, I_{IH}					
INPUT CAPACITANCE					
Data Bus, C_{IN}				pf	
Clock, C_{IN}				pf	
All other, C_{IN}				pf	
DATA BUS LEAKAGE in INPUT MODE					
I_{OB}					
I_{OB}					
POWER SUPPLY CURRENT					
I_{CC}				ma	
I_{DD}				ma	
A.C. CHARACTERISTICS					T_A = 25°C
DOT COUNTER CARRY					
frequency	0.2	4.0		MHz	Figure 1
PW_H	35			ns	Figure 1
PW_L	190			ns	Figure 1
t_r, t_f		10		ns	Figure 1
DATA STROBE					
$PW_{\overline{DS}}$		150		ns	Figure 2
ADDRESS, CHIP SELECT					
Set-up time		100		ns	Figure 2
Hold time		50		ns	Figure 2
DATA BUS—LOADING					
Set-up time		100		ns	Figure 2
Hold time		75		ns	Figure 2
DATA BUS—READING					
T_{DEL2}		100		ns	Figure 2, CL = 50pf
OUTPUTS: HØ-7, HS, VS, BL, CRV, CS-T_{DEL}		100		ns	Figure 1, CL = 20pf
OUTPUTS: RØ-3, DRØ-5					
T_{DEL3}		1.0		μs	Figure 3, CL = 20pf

Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.

2. An even number of scan lines per character row must be programmed in interlace mode. This is again due to pin count limitations which require that the least significant bit of the scan counter serve as the odd/even field indicator.

3. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew between the horizontal address counter and the horizontal blank and sync signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (= 3H).
Vertical Data Start	8 bits assigned providing scan line resolution in vertical data positioning with respect to vertical sync. The Data Row Counter is reset at vertical sync and will not begin counting until the scan line selected by these eight bits.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a Ø1Ø1 address on AØ-3. The device will remain reset at the top of the even field page until a start command is executed by presenting a Ø111 address on AØ-3.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on AØ-3, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the 111Ø address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 11Ø1) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ-7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39, 40, 1, 2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if MSB of Characters/Data Row word is a "1", otherwise output is MSB of Data Row Counter
8	RØ	Scan Counter LSB (Odd/Even Field)	O	Least significant bit of the scan counter. In interlaced mode this bit defines the odd or even field. In this way, odd scan lines of the character font are selected during the odd field and even scans during the even field.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN	Composite Sync	O	Active in non-interlaced mode only. Provides a true RS-170 composite sync waveform.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	Vcc	Power Supply	PS	+5 volt Power Supply
13	VDD	Power Supply	PS	+12 volt Power Supply

Timing Diagrams

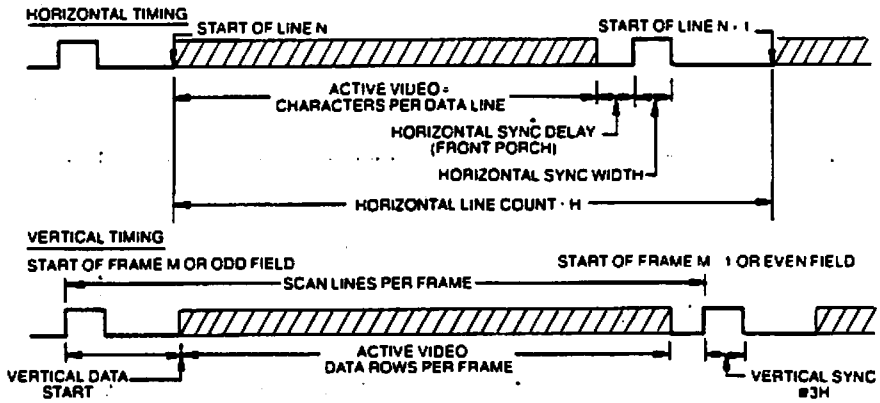
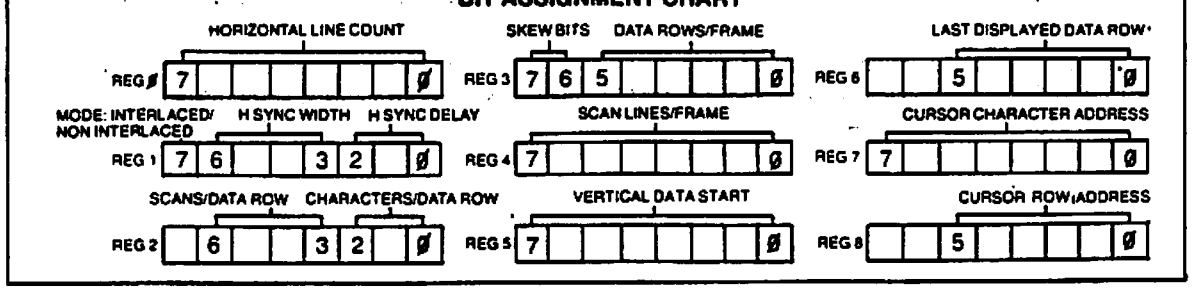


TABLE 1

BIT ASSIGNMENT CHART



Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Self Load	Command from processor instructing CRT 5027 to enter Self Load Mode
1	0	0	0	Read Cursor Character Address	
1	0	0	1	Read Cursor Line Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address	
1	1	0	1	Load Cursor Line Address	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on AØ-3 long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one CRT 5027, the Dot Counter Carry should be held low when this command is removed.

NOTE: During Self Load, the scan counter states corresponding to the nine load command addresses will load the appropriate register. Therefore if reseting of the cursor X and Y position registers is required via self load the PROM words for address 11ØØ and 11Ø1 should be programmed as all zeros.

AC TIMING DIAGRAMS

FIGURE 1 VIDEO TIMING

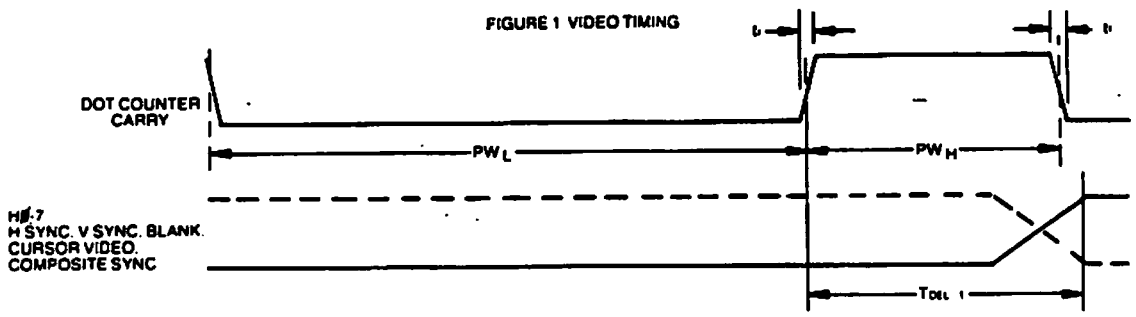


FIGURE 2 LOAD READ TIMING

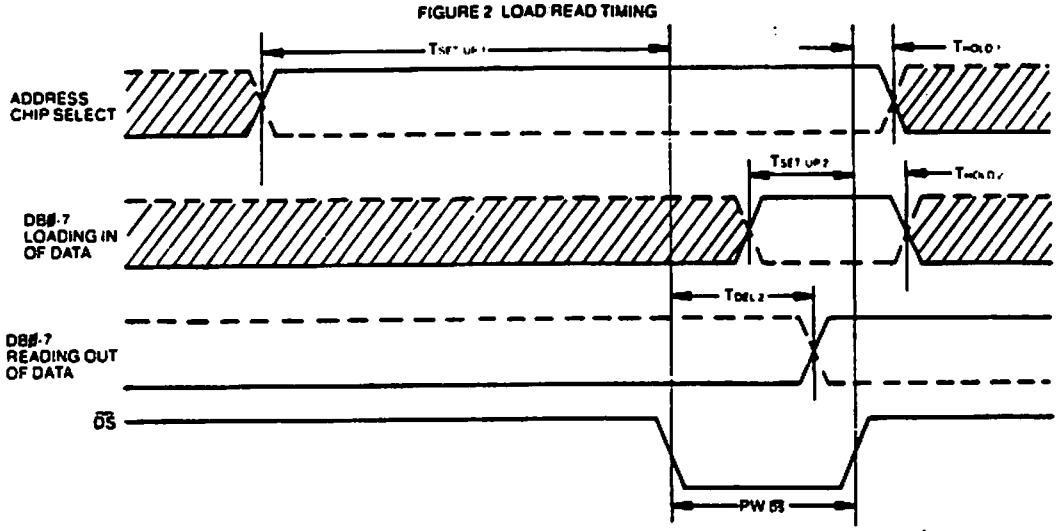


FIGURE 3 SCAN AND DATA ROW COUNTER TIMING

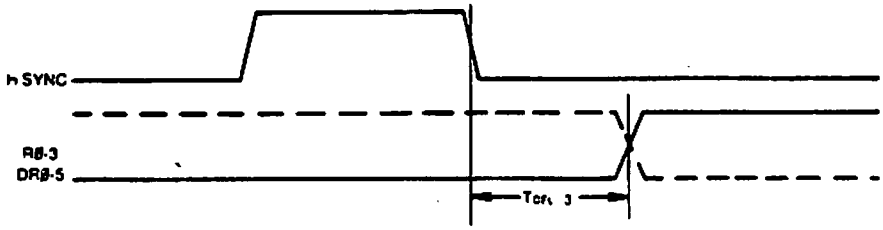
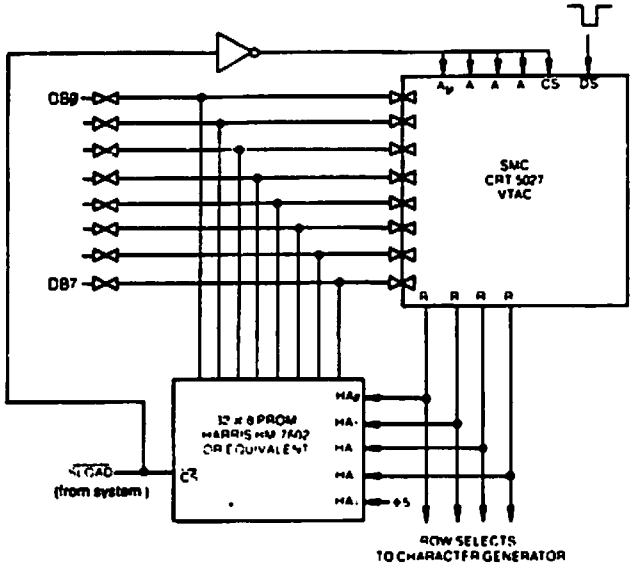


Figure 4. SELF LOADING SCHEME FOR CRT 5027 SET-UP



APPENDIX D

50-PIN BUS

PIN	DESIGNATION	PIN	DESIGNATION
1	+12V (to 250 MA)	26	D2 Bus
2	MR	27	A2
3	MW	28	D3 Bus
4	I/O W	29	A3
5	ø2 (+12V)	30	D7 Bus
6	ø2 TTL	31	A4
7	ø1 (+12V)	32	D6 Bus
8	17.9712 MHz	33	D4 Bus
9	SYNC	34	D5 Bus
10	RESET	35	A6
11	-5V (to 250 MA)	36	D0 8080
12	+5V (to 1 ampere)	37	A7
13	GND	38	D1 8080
14	I/O R	39	A8
15	A10	40	D2 8080
16	READY	41	A14
17	WR	42	D3 8080
18	DBIN	43	D4 8080
19	HOLD	44	A9
20	A5	45	A13
21	A11	46	D7 8080
22	D0 Bus	47	A12
23	A0	48	A15
24	D1 Bus	49	D5 8080
25	A1	50	D6 8080

No more than one TTL load per signal lead.
Maximum load on DC supplies as indicated.

Cable leads to interconnecting device should be kept short -- no more than six inches for some applications.

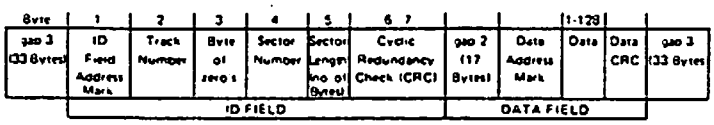
NOTE: The above list applies to the 3621 type Logic Module. For the current X-bus and other connections, see drawing 101815.

Misc.

FLOPPY DISK CONTROLLER APPLICATION NOTE

Introduction

The FD1771 is a MOS/LSI device that performs the function of interfacing a processor to a flexible (Floppy) diskette drive. This single chip replaces nearly 80% of the required disk drive interface electronics. (See figure 1-1). It provides the data accessing controls and the bidirectional transfer of information between the processor's memory and the magnetically stored data on the diskette. The diskette data is stored in a data entry format compatible with the IBM 3740 specification (other formats may be used providing more data storage). In this format all information is recorded on tracks (radial paths) in sectors (arc sections) defined by a programmed header as shown below:



The FD1771 handles single density frequency modulated (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses identifies the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

Index Address Mark	Data	1 1 1 1 1 1 0 0	=FC
	Clock	1 1 0 1 0 1 1 1	=D7
ID Address Mark	Data	1 1 1 1 1 1 1 0	=FE
	Clock	1 1 0 0 0 1 1 1	=C7
Data Address Mark	Data	1 1 1 1 1 0 1 1	=F8
	Clock	1 1 0 0 0 1 1 1	=C7
Deleted Data Address Mark	Data	1 1 1 1 1 0 0 0	=F8
	Clock	1 1 0 0 0 1 1 1	=C7

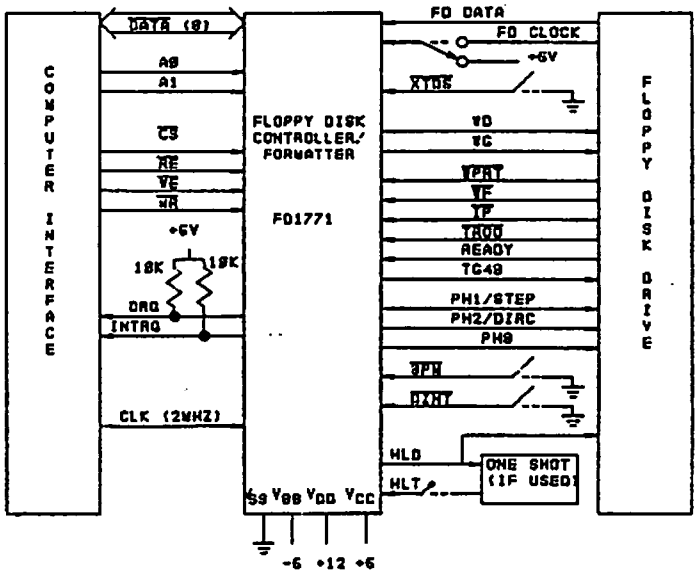
These patterns are used as synchronization codes by the FD1771 when reading data and are recorded by the formatting command, Write Track, when the FD1771 is presented with data F7 through FE.

SECTION I FD1771 DESCRIPTION

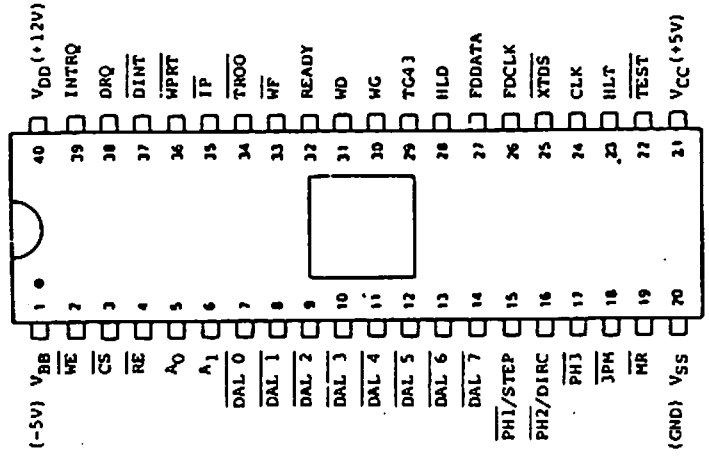
1.1 FD1771 – Flexible Drive Interface (Refer to Figure 1-1 FD1771 Block Diagram)

The FD1771 generates all controls to position the read/write head over the desired track. The FD1771 has the capability of sending successive three phase pulses over the lines PH1, PH2, and PH3 for 3 phase stepping motors or by sending a level over the PH2 line and pulses over the PH1 lines to determine direction and stepping rate for step-direction motors. The particular motor interface is chosen by hardwiring the external pin, 3PM.

ALL REFERENCE TO FD1771 DENOTES FD1771-01 VERSION



FD1771 SYSTEM BLOCK DIAGRAM
FIG 1



A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

3128 RED HILL AVENUE, BOX 2180
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(714) 557-3550 TWX 910-595-1139

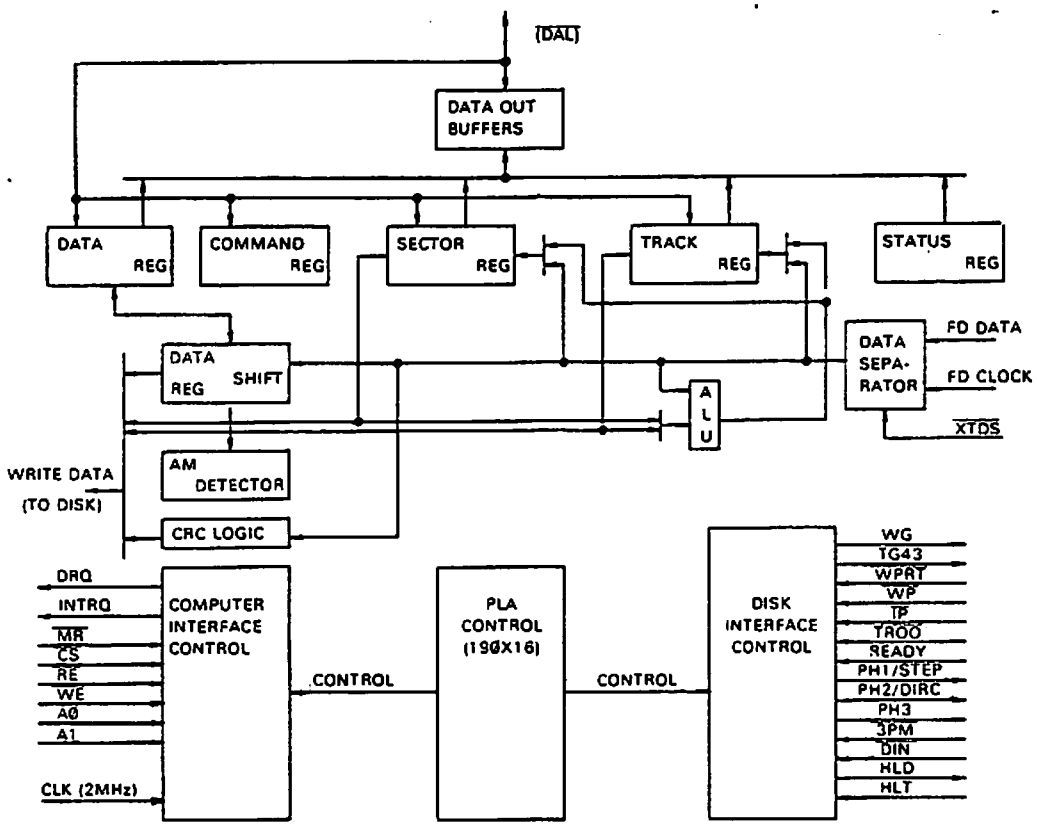

FIGURE 1-1

The head is loaded against the recording media (diskette) by the HLD (Head Load) signal from the FD1771. A read or write operation does not occur until a logic high signal is sampled at the HLT (Head Load Timing) input. This input is sampled after a 10 msec internal delay. This input may be wired high if 10 msec time is sufficient or a one shot may be used to extend this time. If the head is already engaged from a previous operation the resetting of bit 2 in the Read or Write Command (see Processor Interface) will disable the HLT functions and the 10 ms delay.

When reading the serial data from the disk the FD1771 will look for the desired sector to be read, check its ID field and locate its data address mark. All subsequent serial data is assembled in parallel form and presented to the processor interface. The serial data read from the Floppy Driver may be input as composite data, both clock and data present at the FDDATA input, or as separated data in which the data is input to the FDDATA pin and the clock is input to the FD Clock pin.

When writing, information is presented as composite of serial clock and data pulses of 500 nsec periods. With data present at the WD output the WG (Write Gate) signal is activated to allow current to flow in the Read/Write head.

The remaining interface between the FD1771 and the Floppy Drive concerns status information. The $\overline{IP}$ (Index Pulse) and $\overline{TR00}$ (Track 00) signals are outputs of the drive to indicate when the index mark is encountered (once per revolution of the disk) or when the Read/Write head is located over Track 00 respectively.

The $\overline{WPRT}$ (Write Protect), $\overline{DINT}$ (Disk Initialization), and Ready signals reflect the drive condition. The Write Protect signal, when a logic low, prevents the FD1771 from executing a Write Command. The Disk Initialization input, when a logic low, prevents a Write Track Command and essentially disables the rewriting of a format over a previously formatted diskette. The Ready signal indicates Floppy Drive readiness and a logic low on this input prevents any Read or Write command from being exeouted.

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(714) 557-3550 TWX 910-595-1139

Other status interface signals are $\overline{WF}$ (Write Fault) from the Drive which signifies a write operation fault such as failure to detect write current when WG is turned on terminating the Current Write command; and the TG43 signal to the drive indicating the track to be written on is located between Track 44 and Track 76. This latter signal is used by the drive to lower the write current on inner tracks and compensate for the higher density recording of these tracks.

1.2 FD1771 – Processor Interface (See figure 1-1)

All commands, status and data are transferred over the 3 state bidirectional $\overline{DAL}$ (Data Access) lines. These 8 lines present an open circuit to the common processor peripheral bus until activated by the $\overline{CS}$ (Chip Select) signal. An active $\overline{CS}$ combined with $\overline{RE}$ (Read Enable) sets the $\overline{DAL}$ into the transmitter mode while the $\overline{CS}$ combined with an active WE (Write Enable) sets the $\overline{DAL}$ in the receiver mode. The information in the FD1771 resides in 5 accessible 8 bit registers. These registers are: (1) The bidirectional Data Register which acts as a parallel buffer for read or write operations, and receives the desired track number to be accessed in seek operation. (2) the Command register which receives and stores commands from the processor, (3) The sector register which receives the desired sector number to be accessed, (4) The track register which contains the present Track position, (5) The Status Register containing information about the present operation.

The accessing of the registers is accomplished by a combination of active levels on the $\overline{CS}$, $\overline{RE}$, or $\overline{WE}$, and the register address lines A1 and A0. The Command Register can only receive information and the Status Register can only transmit information.

Two signals are available to aid in program response to the FD1771. The INTRQ (Interrupt Request) is activated by the controller whenever an operation is completed successfully or terminated by a fault. The DRQ (Data Request) signal is available as an indication of the chips readiness to transfer a byte of data during read or write operations.

A 2MHZ clock is required by the chip as a reference for all timed signals such as motor controls and data transfers. The $\overline{MR}$ (Master Reset) clears the command register and initiates a Restore (seek track 00) Command when the $\overline{MR}$ line is returned to an inactive state.

1.3 FD1771 Instructions

The FD1771 can be considered a specialized microprocessor with its own instruction repertoire. These are listed in the Tables below.

The Restore, Seek, and the three Step commands position the Read/Write head over the desired track. The Restore positions it over Track 00, the Seek poisitions it over the track specified in the Data Register, and the Step Commands position the head over an adjacent track to its present position.

The Step In moves the head inward toward the center of the disk while the Step Out moves it outward from the center. The Step Command moves the head one step in the same direction as the previous command.

The Read and Write commands are the normally executed commands when transferring information. The Read command initiates a search for a track and sector code in the ID field equal to that in the track and sector registers. When found, the data is formatted from serial to parallel and presented to the Data Register along with the setting of the DRQ signal. By setting of bit 4 in the Read (or Write) command all data records from the desired sector until the last sector on the track are sequentially assembled. The setting of bit 3 allows other combinations of byte count per sector than the standard IBM format.

The Write Command operates similar to the Read Command in multiple sector and variable sector length. All received words in the Data register are transferred to the shift register at which time the DRQ line is set. Four separate Data address marks are selectable through bits 1 and 0 which are written on the diskette prior to writing the sector data.

The Read Address command provides the next encountered ID field (6 bytes) on the diskette to the processor. This can be used to identify the track over which the head resides and can be used if one were to multiplex between two or more drives and wish to return to the first drive. This could also be accomplished by storing the track register in memory and returning it when reactivating the first drive.

The Write Track command is basically used for formatting. Once the index position is located the FD1771 will request data and transfer it to the disk including all ID fields, gaps, and Data fields. Special address marks and the CRC characters are written by detecting certain data patterns. The Read track command allows the reading of the entire recorded pattern on a track including gaps. (Refer to Data Sheet for formatting details)

The final command is the Force interrupt which can be loaded into the Command register at any time. This will terminate any present operation and can also generate an interrupt under four selectable conditions.

1.4 Status Register (See Table 1, page 16)

This register contains status information associated with each of the command instructions. Bit 7 always reflects the Ready condition of the Drive while bit 0 (Busy) always defines the status of the FD1771 concerning present operations.

COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

COMMAND FLAG SUMMARY

TYPE I

h=Head Load flag (Bit 3)

h=1, Load head at beginning
h=0, Do not load head at beginning

V = Verify flag (Bit 2)

V=1, Verify on last track
V=0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

r_1r_0=00, 6ms between steps
r_1r_0=01, 6 ms between steps
r_1r_0=10, 10ms between steps
r_1r_0=11, 20ms between steps

u= Update flag (Bit 4)

u=1, Update Track register
u=0, No update

In general bit 1 reflects the state of the external DRQ signal while bit 2 indicates lost data due to overrun or underrun conditions. The Type 1 or head positioning instructions use bit 1 and 2 as a reflection of the $\overline{IP}$ and $\overline{TROO}$ inputs respectively.

Bit 3 normally indicates the encounterance of a CRC error in the ID or Data fields except for Read Track and Write Track commands in which the CRC is not checked. Bit 4 indicates that the desired track or sector was not correctly located. Bit 6 reflects the $\overline{WP}$ input on Seek and Write Commands and combines with bit 5 to identify the encountered data address mark on the Read command. Bit 5 also indicates the head engaged status on Seek commands and Write fault or Write commands.

TYPE II

m = Multiple Record flag (Bit 4)

m=0, Single Record
m=1, Multiple Records

b = Block length flag (Bit 3)

b=1, IBM format (128 to 1024 bytes)
b=0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)

a_1a_0=00, FB (Data Mark)
a_1a_0=01, FA (Data Mark)
a_1a_0=10, F9 (Data Mark)
a_1a_0=11, F8 (Data Mark)

TYPE III

s = Synchronize flag (Bit 0)

$\bar{s}$=0, Synchronize to AM
$\bar{s}$=1, Do not synchronize to AM

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)

I_0=1, Not Ready to Ready Transition
I_1=1, Ready to Not Ready Transition
I_2=1, Index Pulse
I_3=1, Immediate Interrupt

E=Enable HLD and 10 msec Delay

E=1, Enable HLD, HLT and 10 msec Delay
E=0, Head is assumed Engaged and there is no 10 msec Delay

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1.5 Processor Programming

Some examples of the software control of the Floppy Disk Formatter are shown in the following flow chart. The first example (Figure 1-2) shows the writing of information onto a particular track and sector. The second example (Figure 1-3) shows accessing of information from successive sectors. The third example shows how information may be sought by using Track 00 as a table of contents (Figure 1-4)

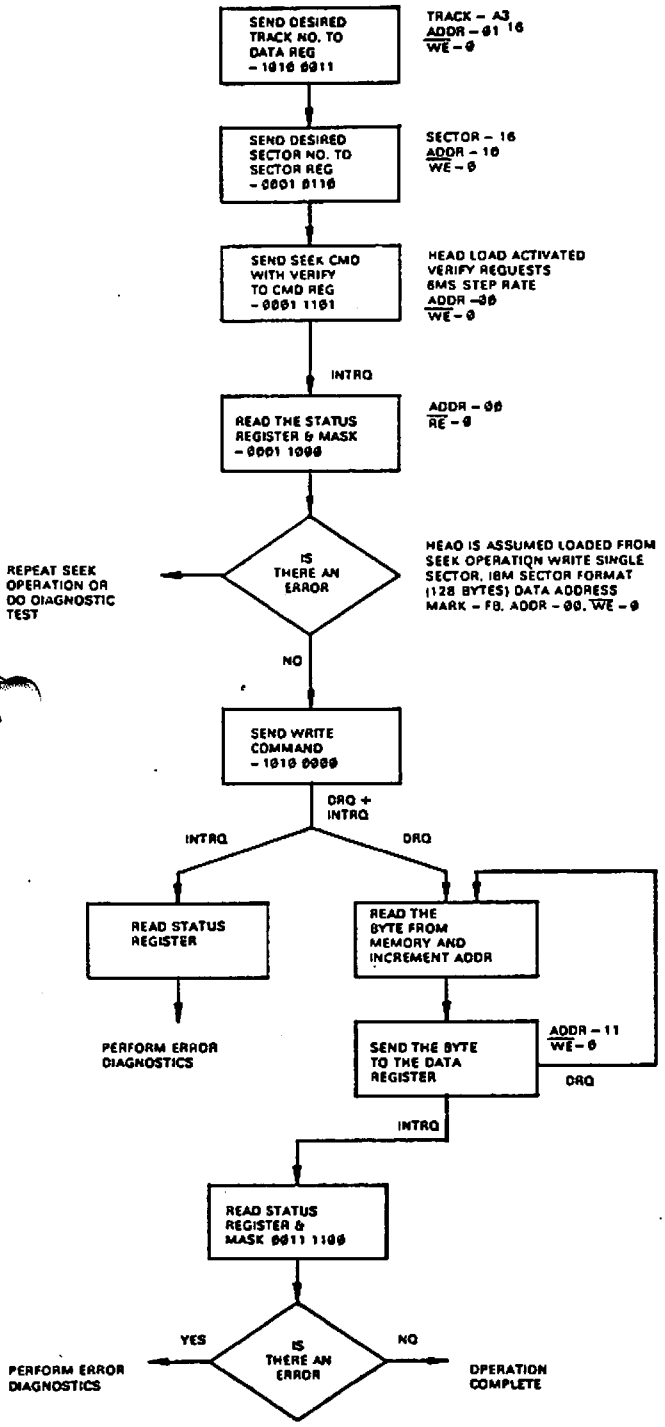

FIGURE 1-2

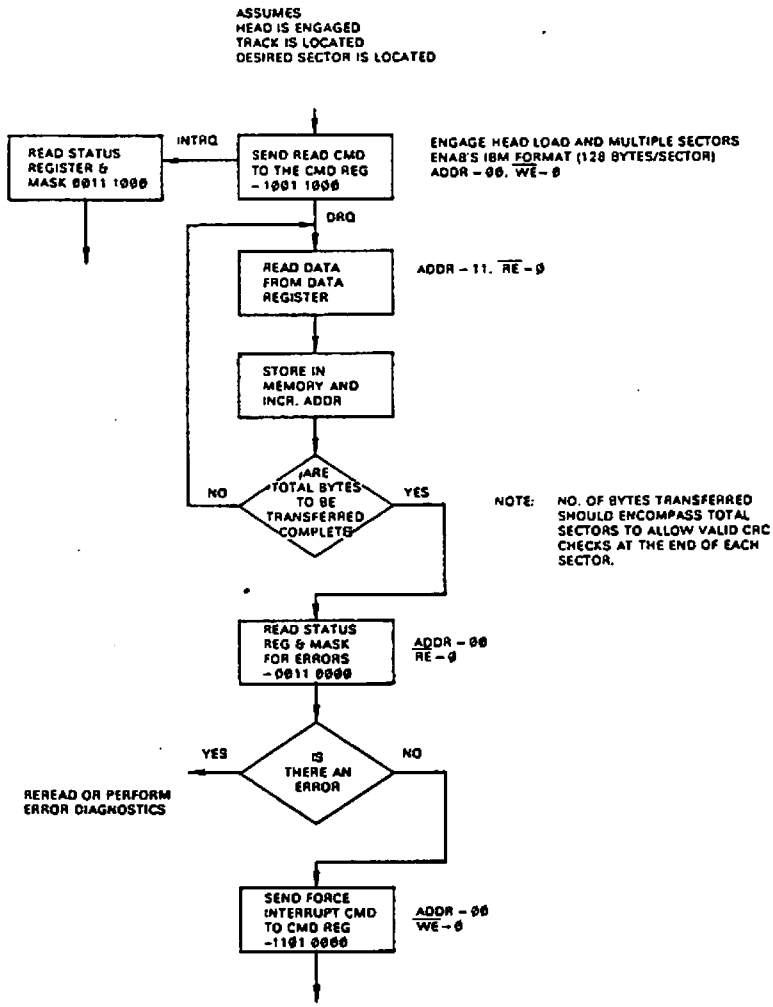

FIGURE 1-3

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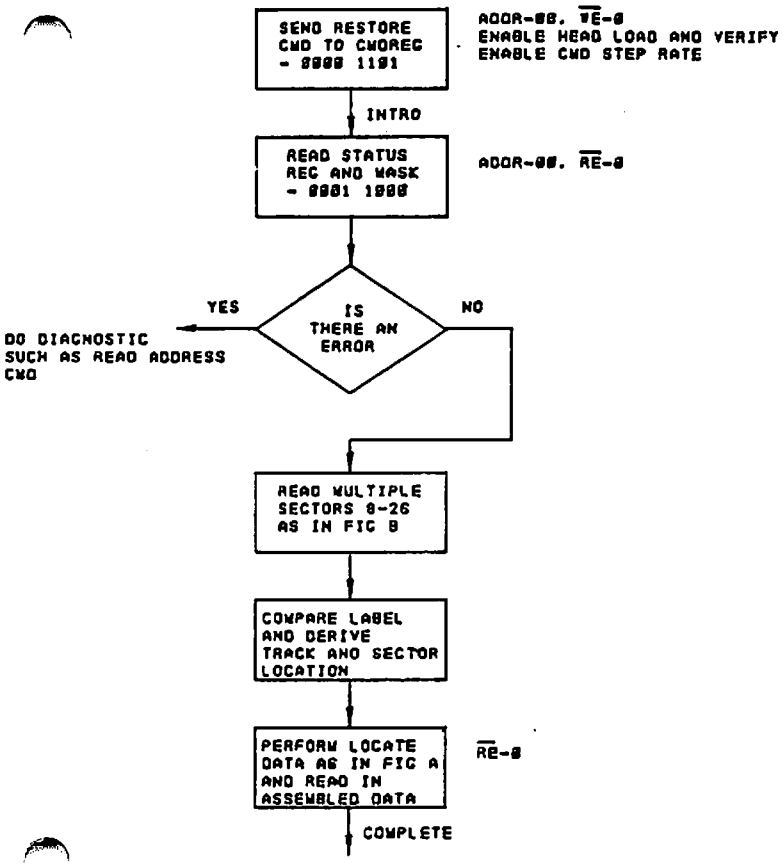

FIGURE 1-4

SECTION II FD1771 INTERFACING

2.1 System Description – Programmed Control

Figures 2-1 to 2-3 demonstrate a possible system configuration for interfacing a processor to a Floppy Disk drive utilizing the FD1771. This configuration requires the proessor to handle all data transfers which will occur as every 32 μsec.

The chip is selected by addressing it through a pre-assigned address. The lower two bits of this address selects which register is to receive or send data. The Read Enable and Write Enable strobes control the data exchange. The clock may be derived on the board or taken from other processor circuits. Generally the outputs of the FD1771 must be interfaced with drivers and receivers to provide proper matching circuits with the drive. One shots may be necessary to meet the drive's required control signal pulse widths. These circuits must be derived from recommended interfaces specified in Drive manufacturers manuals.

A clock and data separator recommended by Motorola is shown in Fugure 2-3A. This phase lock loop (PLL) circuit operates with an internal clock operating at 8MHZ or thirty two times the frequency of a received bit cell. The MC4024 is a Voltage Controlled Multivibrator that supplies the basic clock frequency. The 74LS161 counter A provides a division by 16 and supplies a carry to one side of the MC4044 phase detector. The other input to the MC4044 comes from the 74LS161 counter E carry which is affected by incoming data. The output of the phase detector is a signal proportional to the differences between the incoming pulses. This is fed through a low pass filter (for long term stability) to the input of the 4024 to control the system frequency.

The incoming raw data is shaped through a schmitt trigger and creates a pulse via flipflops G and H each time a clock or data bit is received. These pulses are stretched to 250 nsec by the one shot J and fed to nand gates. The signals are nanded with a data window or clock window and result in separated data and clock outputs.

The separator windows are formed by counter E which clocks the flip flop F at each 8 count and normally provides a 50% window every 2 μsec. Each time a bit is received it will load a count of 9 into this counter. If the system clock frequency is correct this will not alter the count. If the clock is not concurrent with information the count will be advanced or set back to alter the window and change the carry output timing.

The function of the counter D and flip flop F is to provide the proper phasing for separation of data and clock. It accomplishes this task by looking for missing clocks and data. If no clock is detected in four transitions of the OD output of counter E the output OC causes the flip flop to reverse the sampling windows.

Figures 2-3B and 2-3C illustrate two other methods of clock and data separation. The method in 2-3B incorporates a simple clock counter circuit and phasing logic. Figure 2-3C incorporates a one-shot method.

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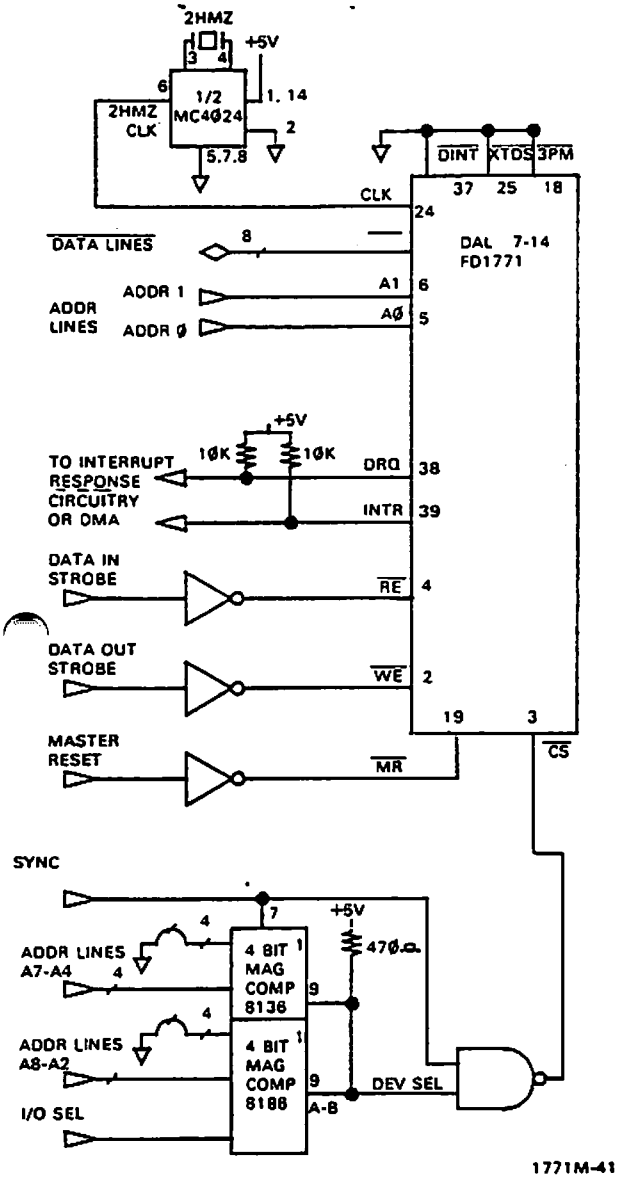

FIGURE 2-1

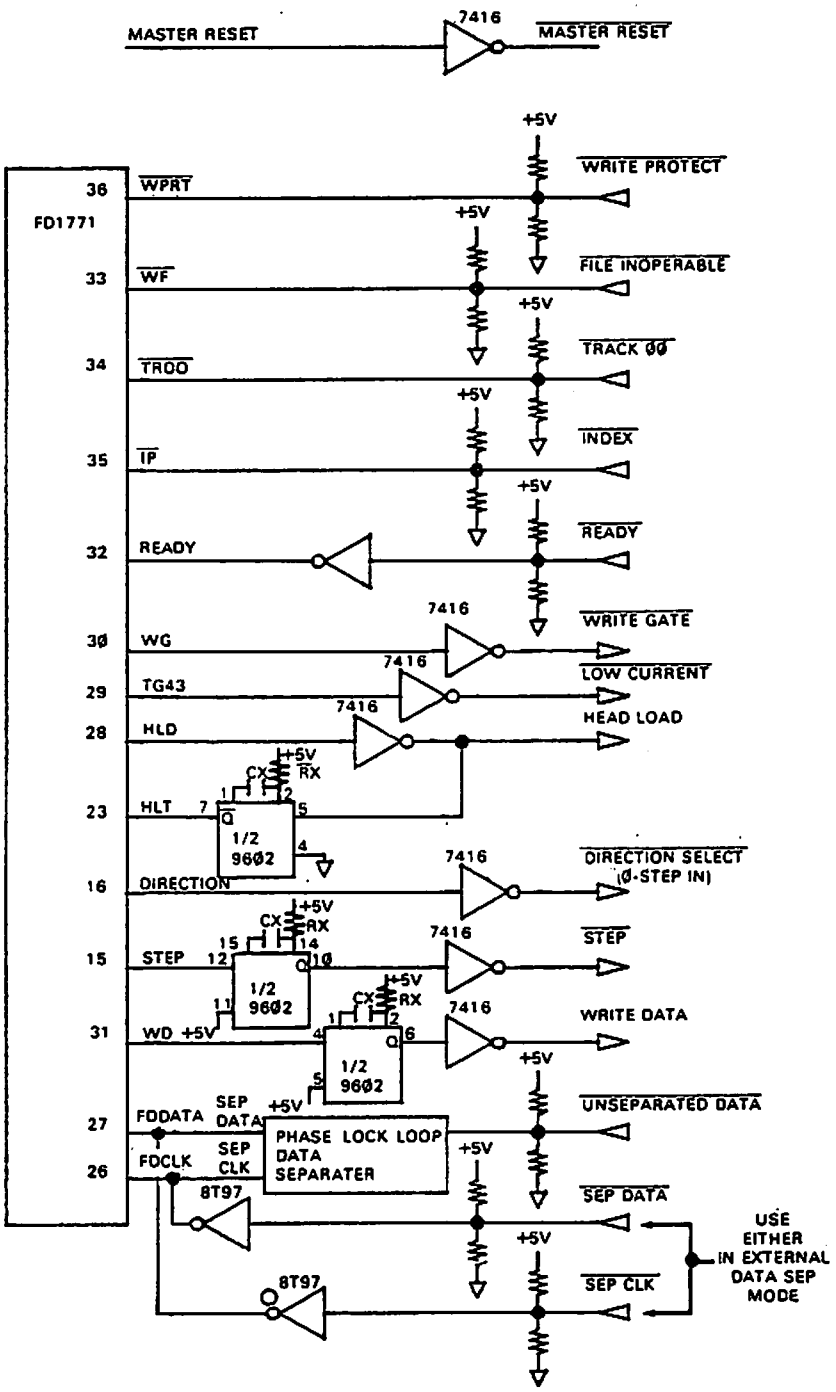

FIGURE 2-2

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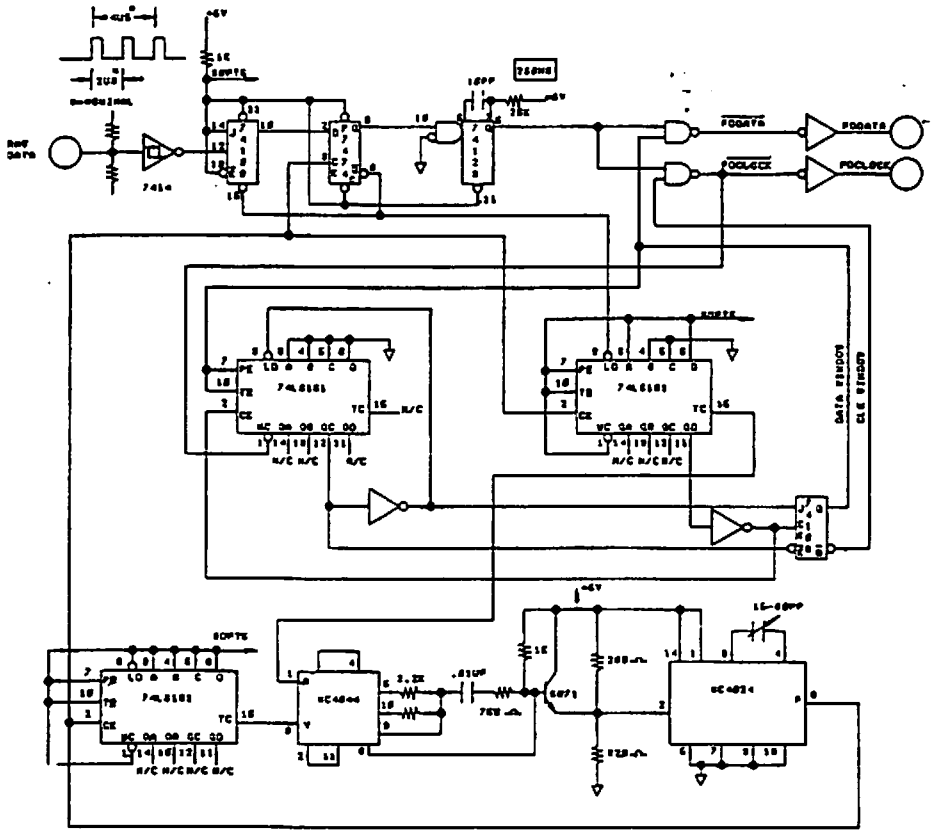
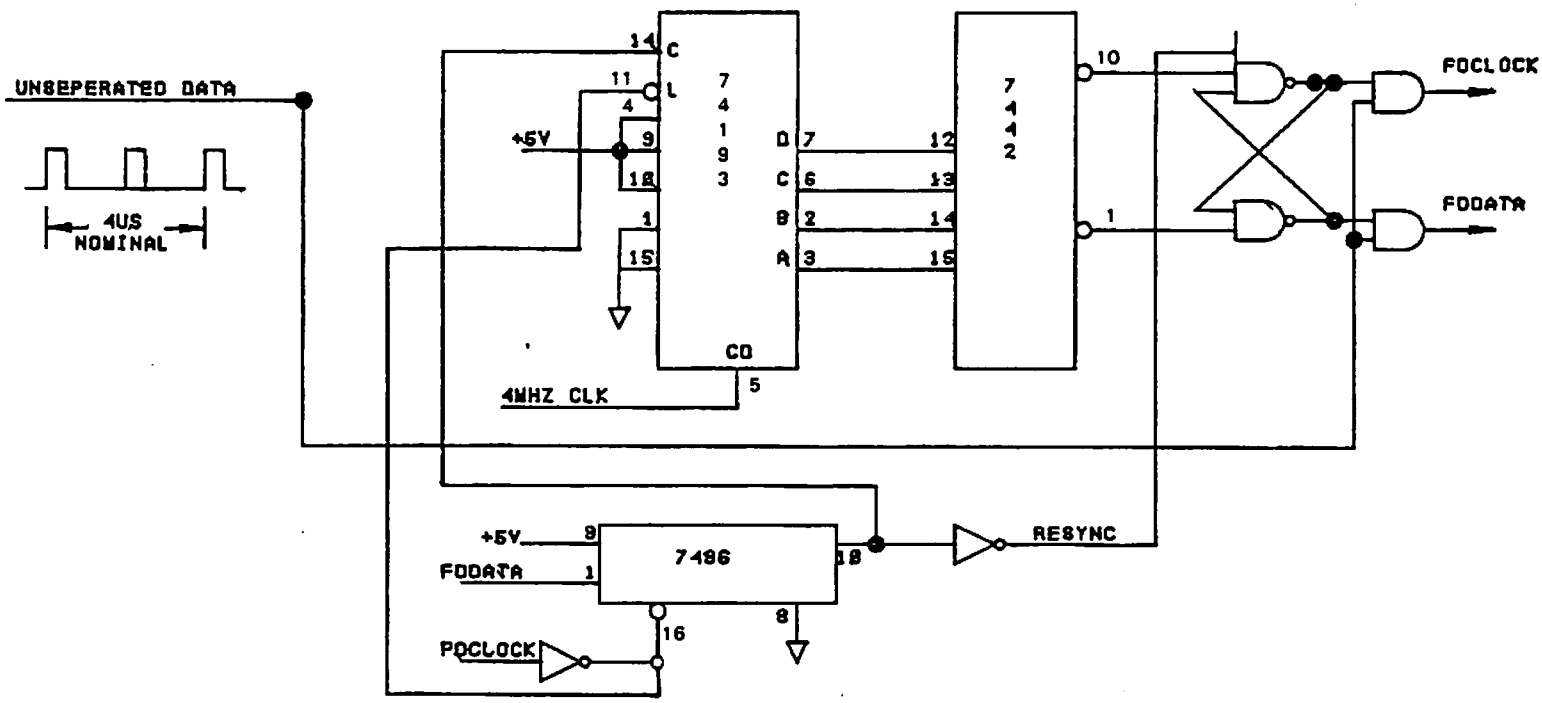


Circuit provided courtesy of Motorola and iCOM Corps.
FIGURE 2-3A



Circuit provided courtesy of Processor Applications Ltd, 2801 E. Valley View, West Covina, Ca. 91792 (213) 965-8865
FIGURE 2-3B

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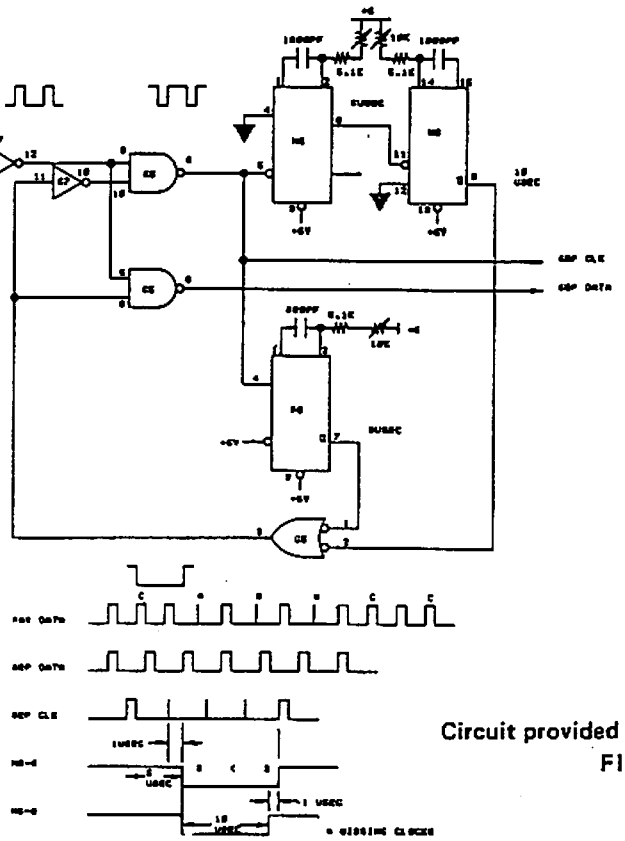

Circuit provided courtesy of Acutest Corp.

FIGURE 2-3C

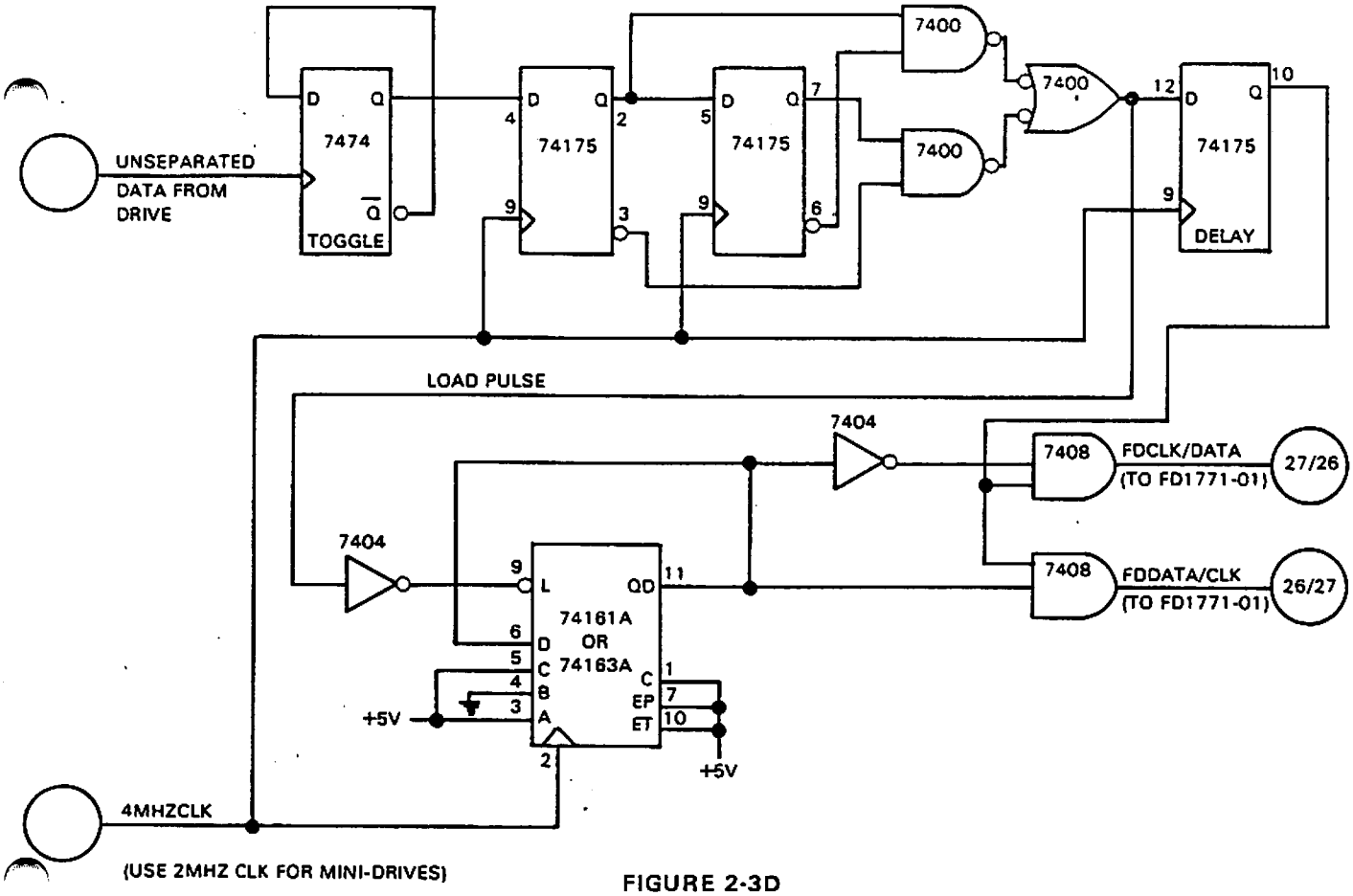

FIGURE 2-3D

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2.2 System Description – Sector buffered

In paragraph 1.1 a program controlled interface was described for the FD1771. This method uses the least number of external IC's but suffers in performance due to the necessity the processor to service the FD1771 every 32 μsec when transferring data to or from the floppy. It may not be possible for some micro-processors to execute the program loop, within 32 μsec, therefore an alternate method of data transfer must be employed. One such method is to buffer the data transfers in a memory device, thereby requiring the processor to service only interrupt requests.

The block diagram in Figure 2-4 shows the FD1771 interface a FIFO buffer. The buffer consists of 4 FR1502 devices which provide 40 characters by 9 bits each for a total buffer storage of 160 bytes. The select logic provides proper data and command steering for block transfers or program control. The select logic will allow the processor to set a load FIFO mode, transfer a sector of information into the FIFO at processor speed, set the FIFO dump mode and send a write command to the FD1771. The data is then transferred at the rate required by the FD1771. Figure 2-5 shows the interface control and timing in the FIFO to FD interface.

When the floppy disk is to be read the processor sets the load FIFO mode and sends a Read command to the FD1771. The FD1771 then transfers data to the FIFO and interrupts the processor when a sector of information has been loaded into the FIFO. The processor will respond to the interrupt by setting the FIFO to the dump mode and then may read the data from the FIFO at processing speeds. Figure 2-6 shows the logic and timing for the FD1771 to FIFO interface.

Figure 2-7 shows the detailed logic for generating the proper control signals to the FIFO and FD1771. Figure 2-8 shows the proper connection for the FR1502 FIFO buffer memory.

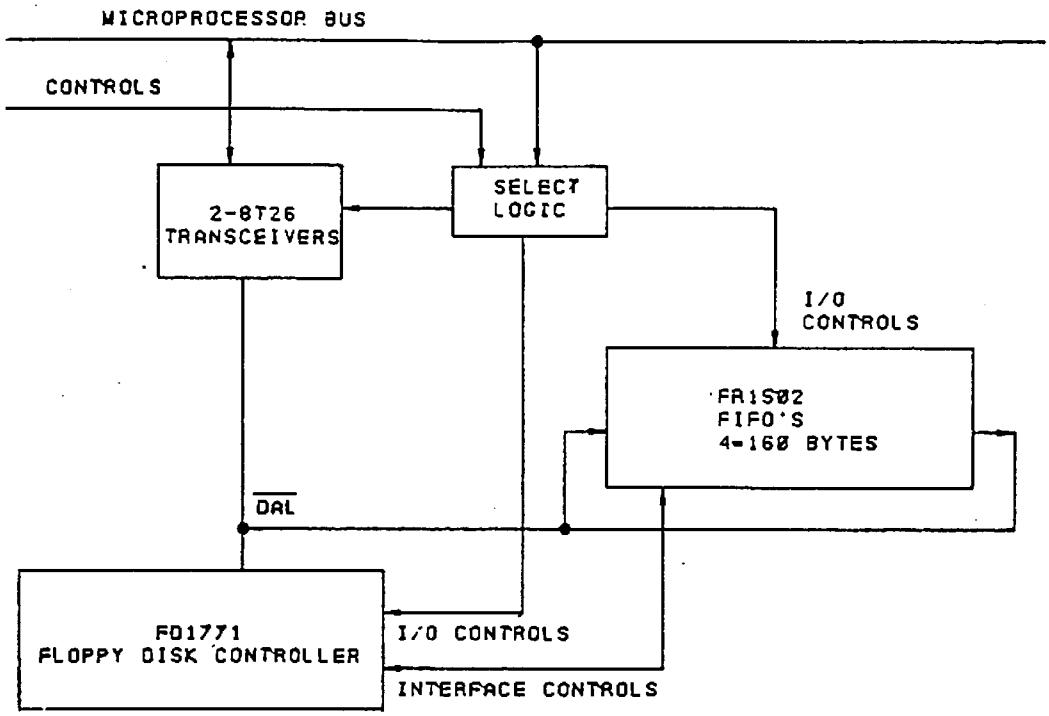
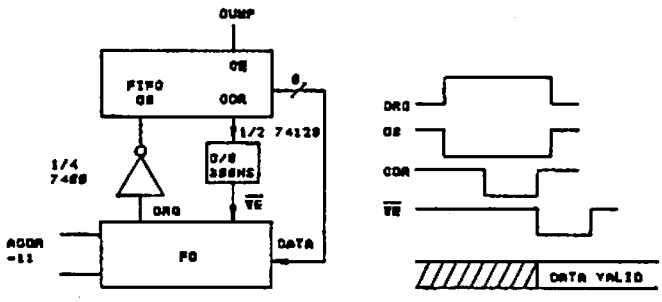
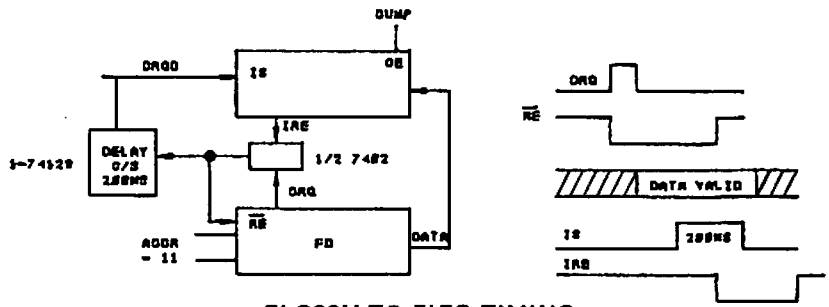


FIGURE 2-4
SECTOR BUFFER BLOCK DIAGRAM



FIFO TO FLOPPY TIMING
FIGURE 2-5



FLOPPY TO FIFO TIMING
FIGURE 2-6

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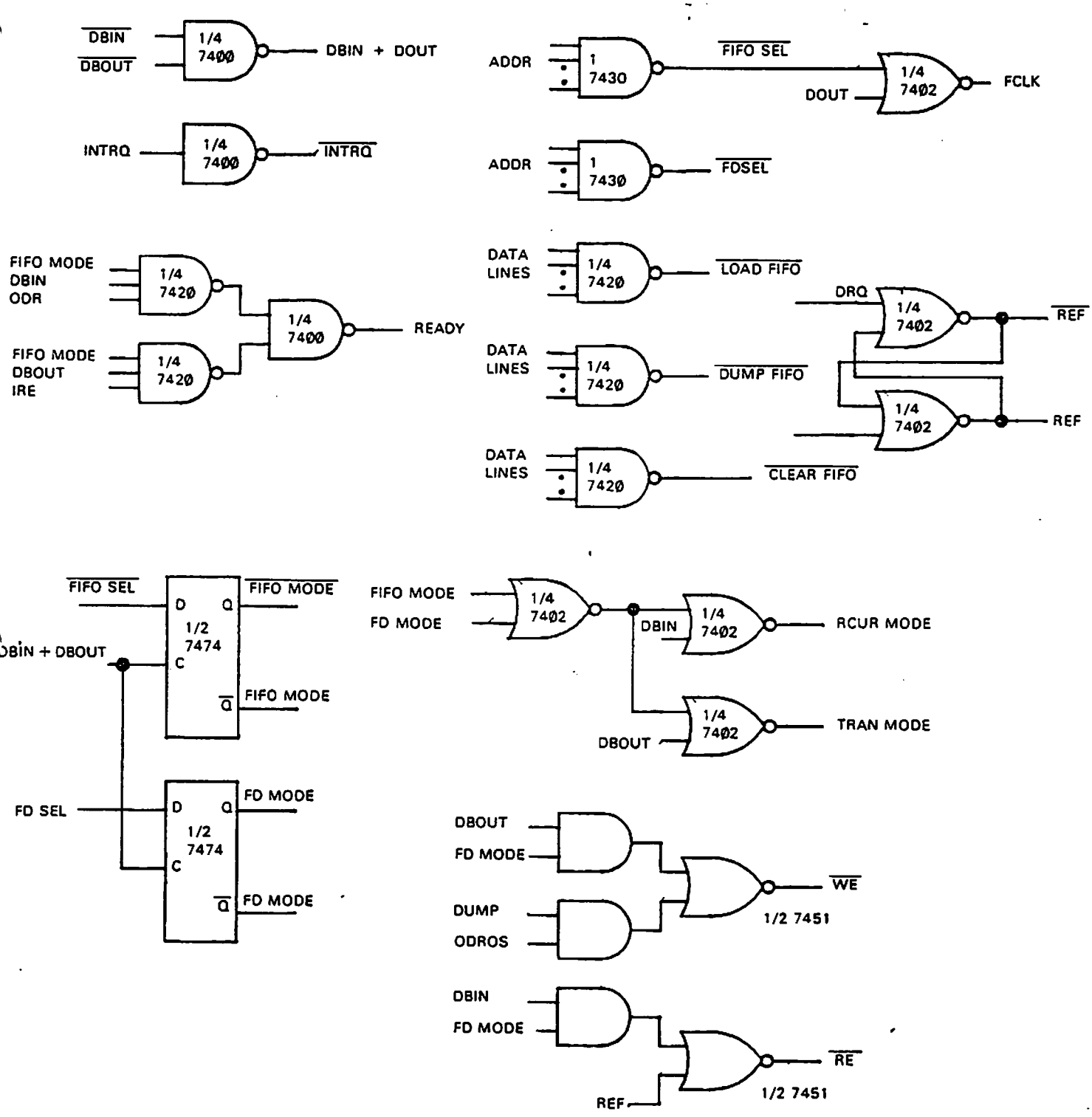

FIGURE 2-7
TIMING CONTROL

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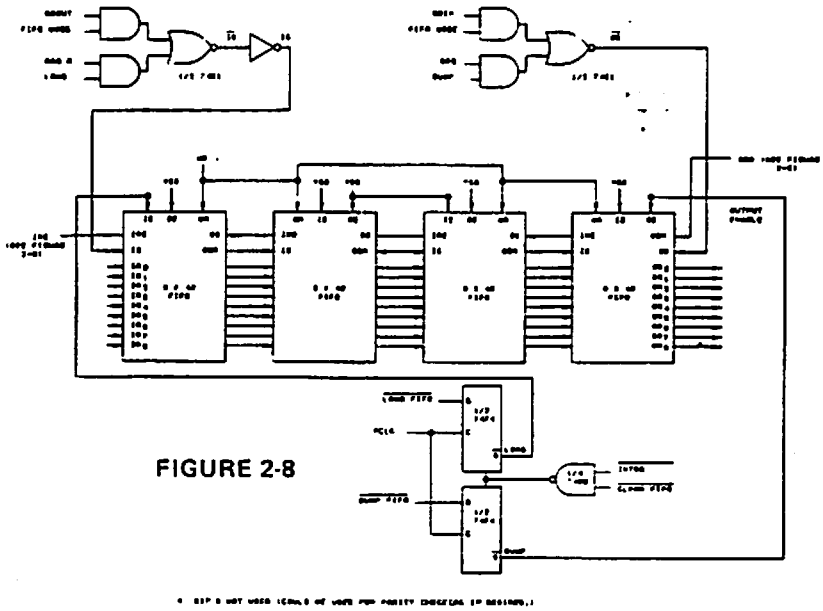

FIGURE 2-8

The format of the Status Register is shown below:

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table below.

YOUR LOCAL WDC REPRESENTATIVE IS:

STATUS REGISTER SUMMARY						
BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

TABLE 1

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{BB} (Ground)	+20 to -0.3V
Max Voltage to Any Input with Respect to V_{BB}	+20 to -0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ±.6V, V_{BB}=-5.0±.5V, V_{SS} = 0V, V_{CC} = +5V ± .25V

V_{DD} - 10ma Nominal, V_{CC} = 30 ma Nominal, V_{BB} = 0.4 ua Nominal

* For complete electrical specifications see FD1771 Data Sheet.

All diagrams within this application note are shown for illustrative purposes & may not necessarily reflect the total logic to implement interface method.

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WESTERN DIGITAL
MOS/LSI

FD1781 A/B

FLOPPY DISK FORMATTER/CONTROLLER

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
- READ MODE
  - Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- WRITE MODE
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Selectable Head Settling and Head Engage Times
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers Comprehensive Status Information

APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
NEW MINI-FLOPPY CONTROLLER

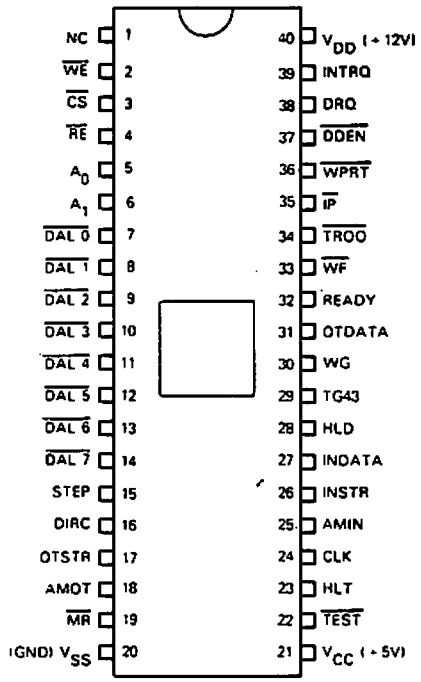
GENERAL DESCRIPTION

The FD1781 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accommodates the interface signals from most drive manufactures. When in the single density mode the FD1781 is fully IBM-3740 compatible. In the double density mode, the type of encoding scheme is a function of the user's data recovery circuits. In this manner both M²FM or MFM is obtainable.

The processor interface consists of a 8-bit bi-directional bus for data, status, and control word transfers. The FD1781 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1781 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.

PIN CONNECTIONS



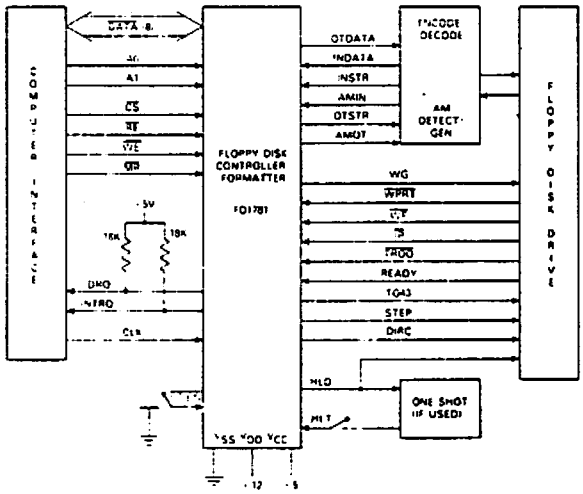
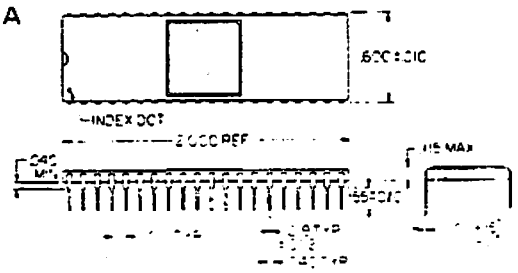


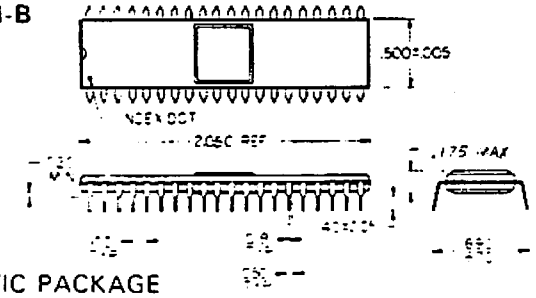
FIG. 1. 1781 SYSTEM BLOCK DIAGRAM

FD1781-A



CERAMIC PACKAGE

FD1781-B



PLASTIC PACKAGE

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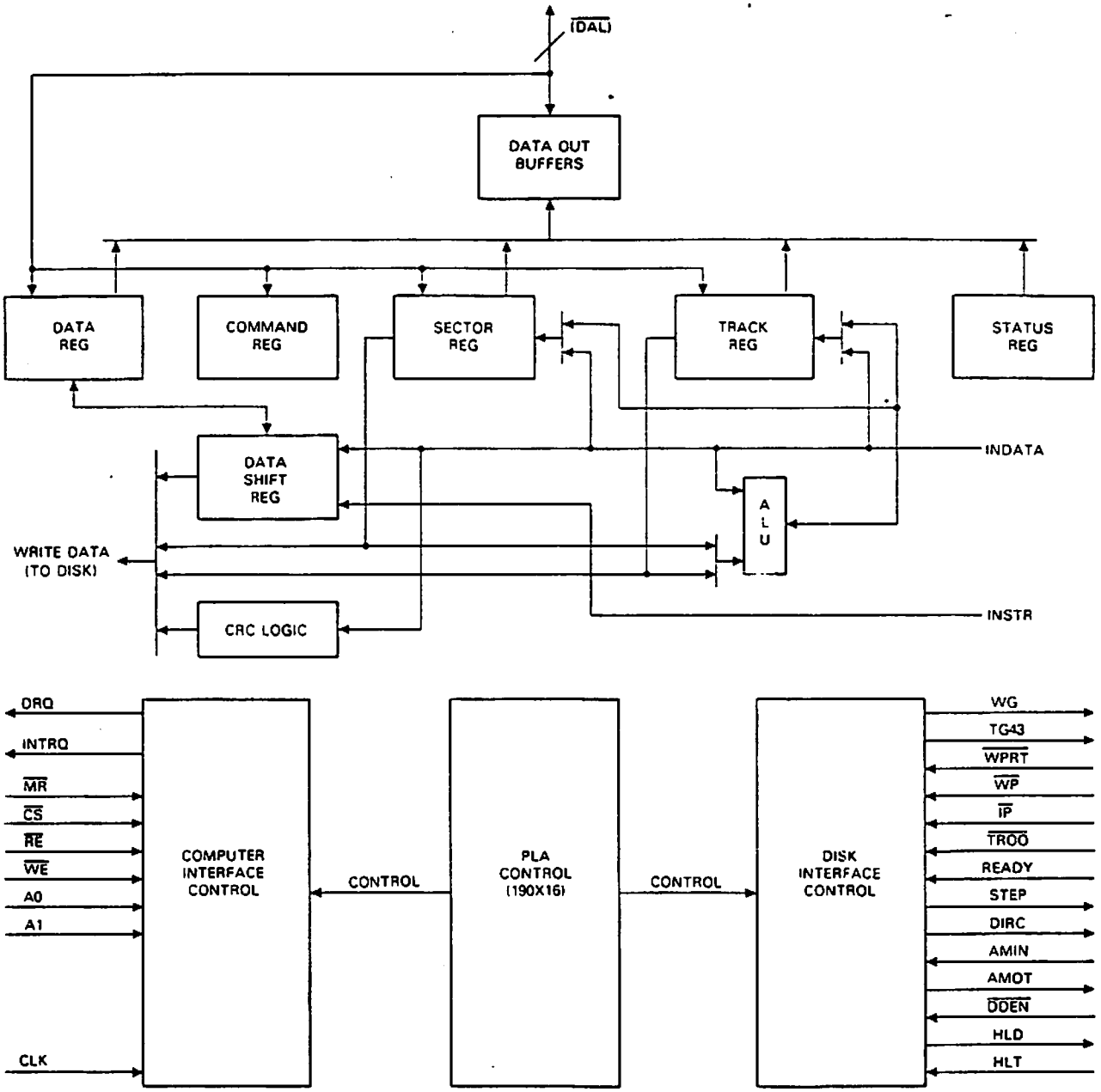

FIG. 3. FD1781 BLOCK DIAGRAM

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated above. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (INDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

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Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1781 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density is assumed. When $\overline{DDEN}$ = 1, single density is assumed. During disk read operations, the user must provide both data recovery and address mark detection circuits external to FD1781 in both single and double density modes. Thus for disk read operations, the user must provide as an input to the FD1781 Data (INDATA) a strobe to indicate when the data is valid (INSTR) and address mark detect (AMIN). During disk write operations and in the double density mode, the FD1781 provides as outputs Data (OTDATA), a strobe to indicate validity (OTSTR) and Address Mark Out (AMOT). During disk write operation and in the single density mode, OTSTR becomes Write Data (WD) which is exactly the same as in the FD1771.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1781. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least-significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1781 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

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On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. The Clock (CLK) input is normally a free-running 2 MHz ±1% when in the double density mode and 1 MHz ±1% when in the single density mode. However when using a mini-floppy, the CLK is normally 1 MHz when in double density mode and 1/2 MHz when in the single density mode.

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step — A 2 μs pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC) — The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is preset.

TABLE 1
STEPPING RATES

CLK	2 MHz	1 MHz	1 MHz	1/2 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1		
R1 R0	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 0	$\overline{TEST}$ = 0
0 0	3 ms	3 ms	6 ms	6 ms	Approx.	Approx.
0 1	6 ms	6 ms	12 ms	12 ms	400 μs	800 μs
1 0	10 ms	10 ms	20 ms	20 ms		
1 1	20 ms	20 ms	40 ms	40 ms		

The Head Load (HDL) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HDL signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input every 10 msec. A high logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read Track and Write Track commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can

be read or written in Read or Write commands respectively by setting a logic 0 in Bit of the command word. The sector length indicator specifies the number of 16 byte groups or 16 × N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1781 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the $\overline{\text{Write Protect}}$ status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1781 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the $\overline{\text{Write Gate}}$ output becomes inactive.

Whenever a Read or Write command is received the FD1781 samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the Ready input.

COMMAND DESCRIPTION

The FD1781 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page four.

TABLE 2
COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\overline{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 3
FLAG SUMMARY

TYPE I

h = Head Load Flag (Bit 3)
- h = 1, Load head at beginning
- h = 0, Do not load head at beginning

V = Verify flag (Bit 2)
- V = 1, Verify on last track
- V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)
- Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u = 1, Update Track register
- u = 0, No update

TABLE 4
FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)
- m = 0, Single Record
- m = 1, Multiple Records

b = Block length flag (Bit 3)
- b = 1, IBM format (128 to 1024 bytes)
- b = 0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)
- a_1a_0 = 00, FB (Data Mark)
- a_1a_0 = 01, FA (User defined)
- a_1a_0 = 10, F9 (User defined)
- a_1a_0 = 11, F8 (Deleted Data Mark)

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TABLE 5
FLAG SUMMARY

TYPE III
s = Synchronize flag (Bit 0)
$\overline{s}$ = 0, Synchronize to AM $\overline{s}$ = 1, Do Not Synchronize to AM
TYPE IV
Ii = Interrupt Condition flags (Bits 3-0)
I0 = 1, Not Ready to Ready Transition I1 = 1, Ready to Not Ready Transition I2 = 1, Index Pulse I3 = 1, Immediate interrupt
E = Enable HLD and 10 msec Delay
E = 1, Enable HLD, HLT and 10 msec Delay E = 0, Head is assumed Engaged and there is no 10 msec Delay

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1781 receives a command that specifically disengages the head. If the FD1781 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the nex encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the FD1781 terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is samples. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1781 terminates operation, interrupts, and sets the Seek error status

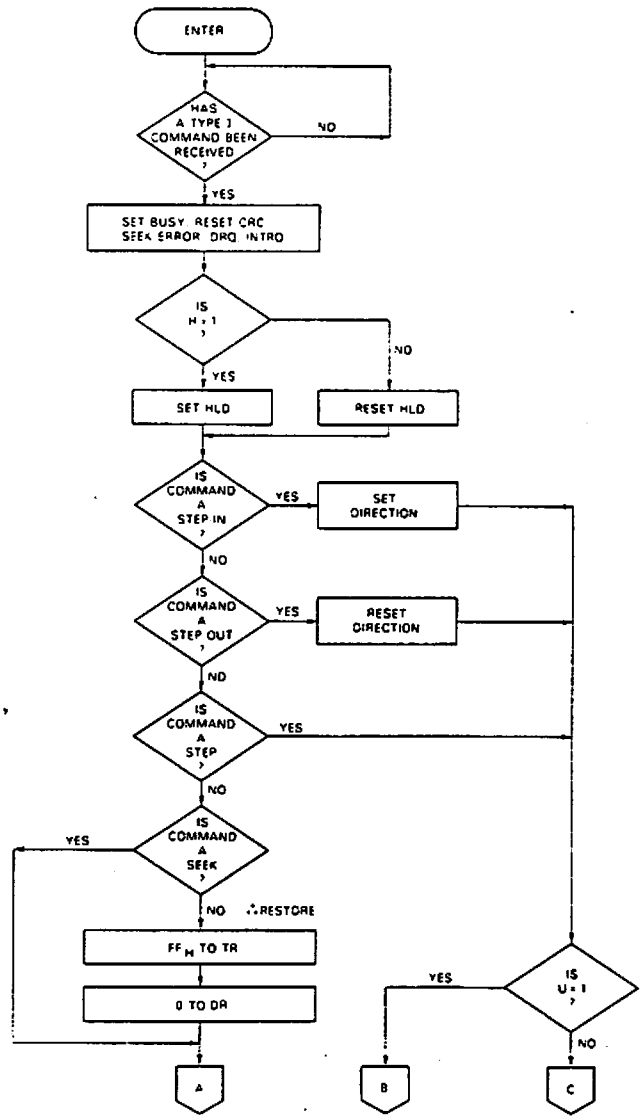

FIG. 4. TYPE I COMMAND FLOW

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bit. Note that the Restore command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1781 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

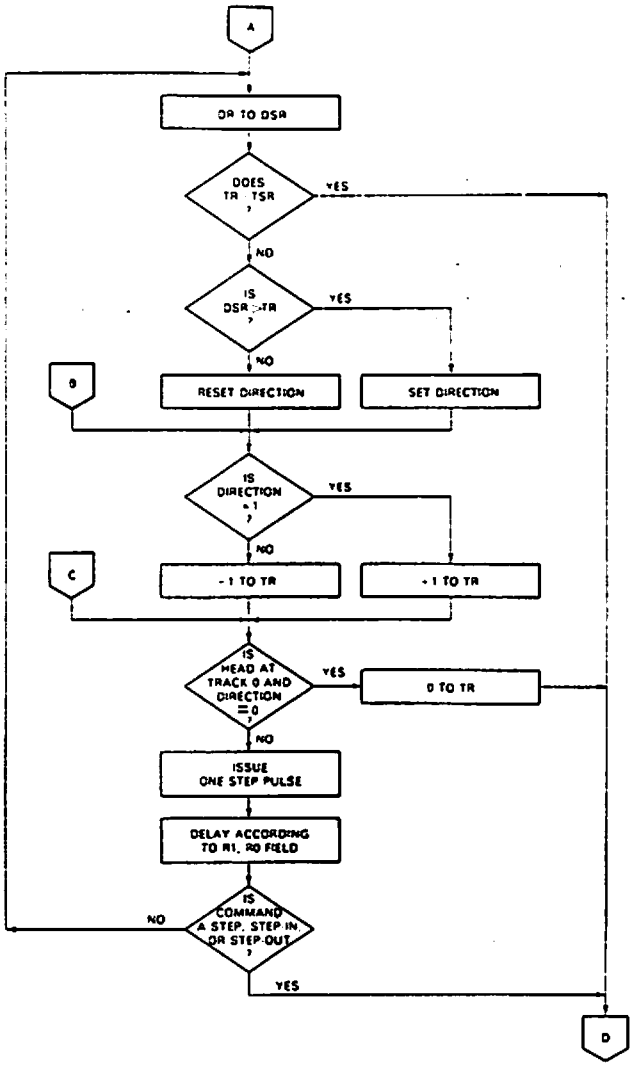


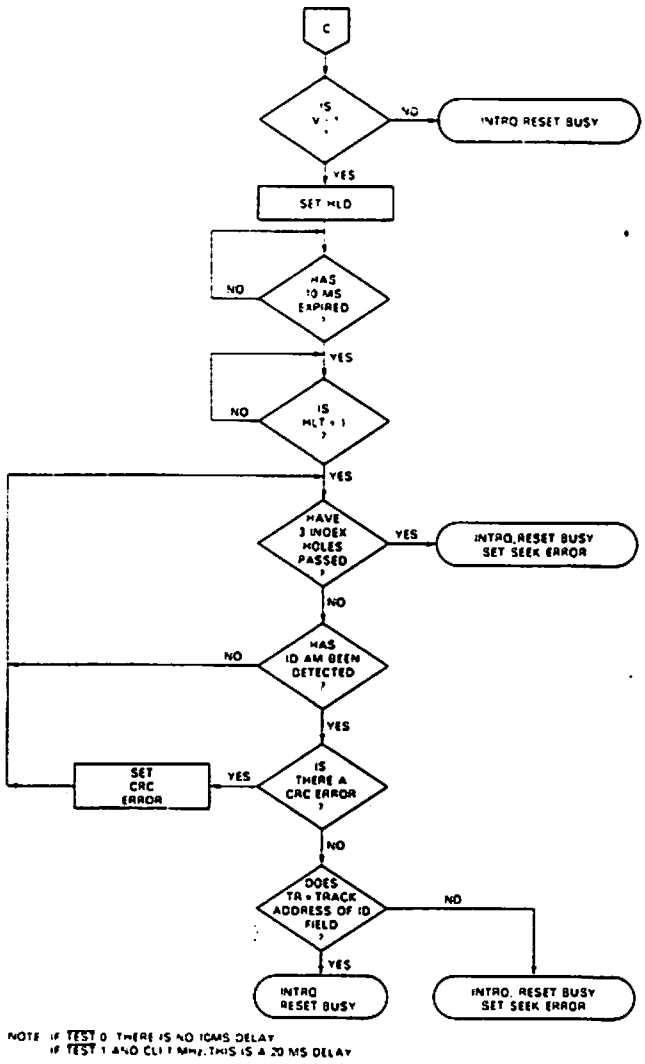
FIG. 5. TYPE I COMMAND FLOW

STEP

Upon receipt of this command, the FD1781 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.



NOTE: IF TEST 0, THERE IS NO 10MS DELAY
IF TEST 1 AND CLK 1 MHz, THIS IS A 20 MS DELAY

FIG. 6. TYPE I COMMAND FLOW

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STEP-OUT

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II Command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and Data Field format are shown below:

When an ID field is located on the disk, the FD1781 compares the Track Number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1781 must find an ID field with a Track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where $n = 0,1,2,3$.

For b = 1

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II Commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0 a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1781 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminated the command and generates an interrupt.

READ COMMAND

Upon receipt of the Read command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the corrected field; if not, the Record Not Found status bit is set and the operation is terminated.

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	1	2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark — DATA = $(FE)_{16}$ CLK = $(C7)_{16}$
Data AM = Data Address Mark — DATA = (F8, F9, FA, or FB), CLK = $(C7)_{16}$

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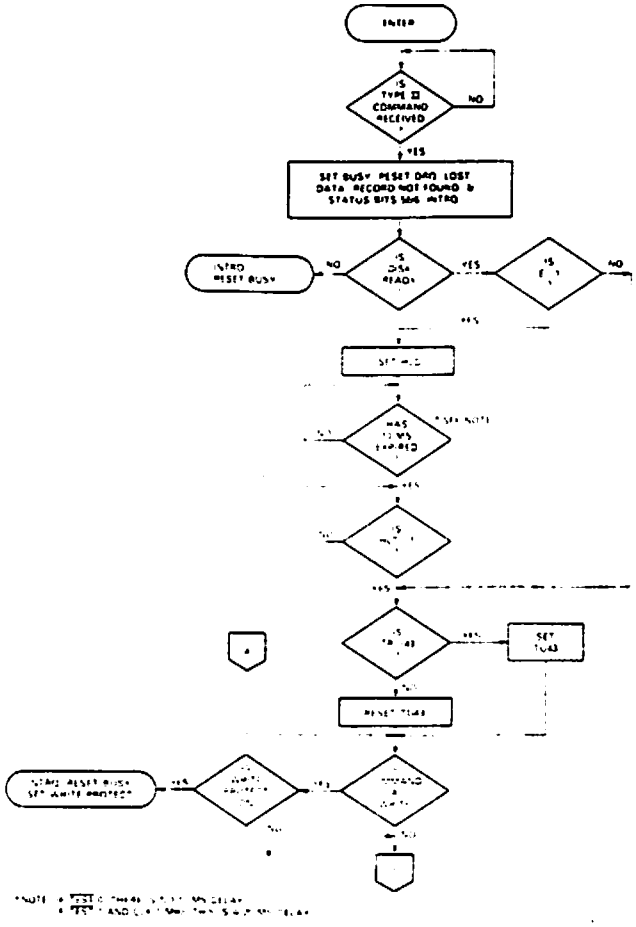

FIG. 7. TYPE II COMMAND

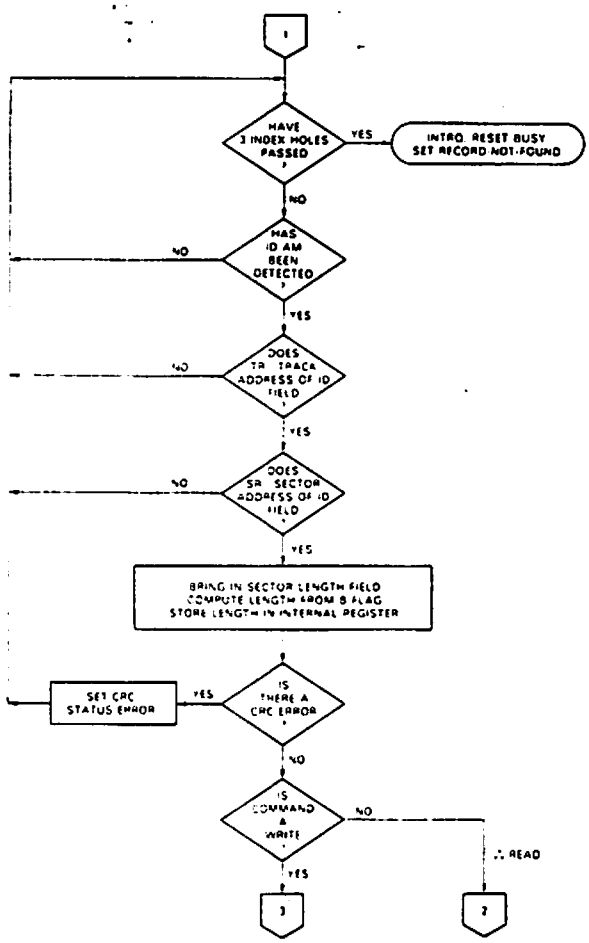

FIG. 8. TYPE II COMMAND

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

STATUS BIT 5	STATUS BIT 6	DATA 1	DATA 2	DATA 3
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	1	1

WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1781 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a^1a^0 field of the command as shown below:

a^1	a^0	DATA 1	DATA 2	DATA 3
0	0	0	0	0
0	1	0	0	0
1	0	1	1	0
1	1	0	1	1

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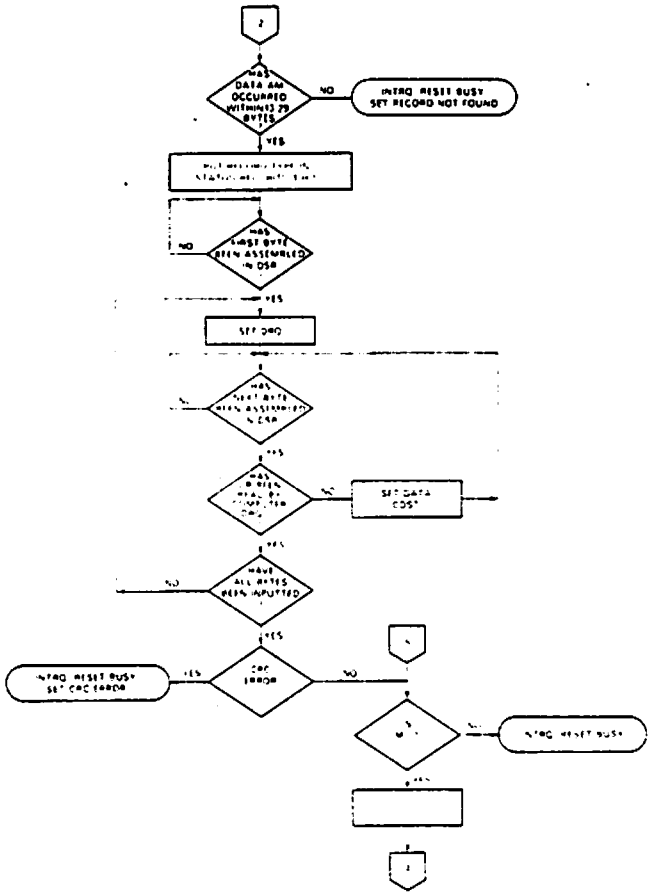

FIG. 9. TYPE II COMMAND

The FD1781 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

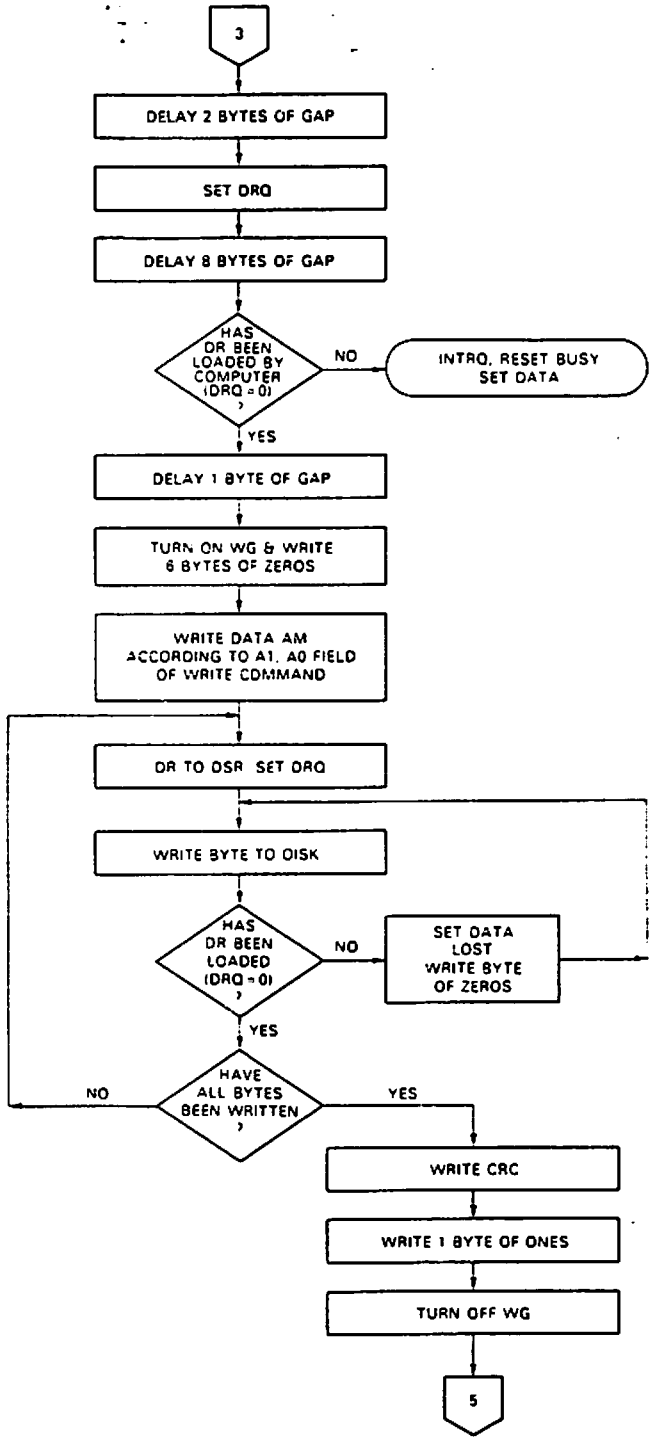

FIG. 10. TYPE II COMMAND

Although the CRC characters are transferred to the computer, the FD1781 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

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READ TRACK

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0 (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

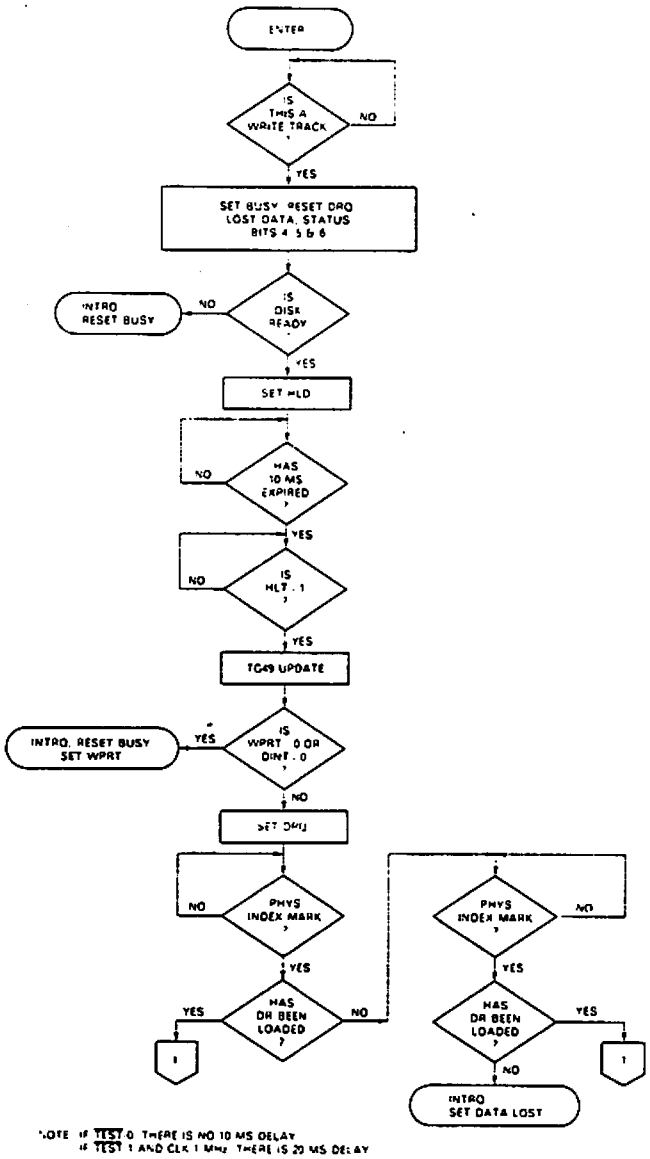

FIG. 11. TYPE III COMMAND WRITE TRACK

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK* (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

*Single density only

DATA 1	DATA 2	DATA 3	TYPE OF ADDRESS MARK
0	0	0	Deleted Data mark
0	0	1	Data Mark (user defined)
0	1	0	Data Mark (user defined)
0	1	1	Data Mark
1	0	0	Index Address Mark
1	0	1	Undefined
1	1	0	ID Address Mark
1	1	1	Undefined

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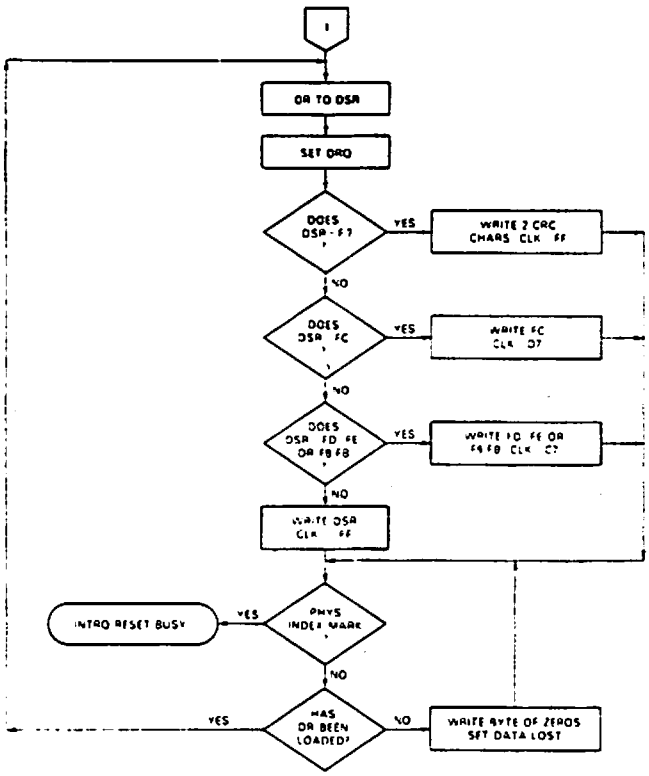

FIG. 12. TYPE III COMMAND WRITE TRACK

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

NOTE: If I_0-I_3 = 0, there is no interrupt generated but the current command is terminated and busy is reset.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

TABLE 6
STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 Not Ready	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 RECORD TYPE/ WRITE PROTECT	On read Record: In indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

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FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1781 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1781 detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7). and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 FORMATS—128 BYTES/SECTOR

Shown in Figure 13, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	00 or FF
6	00
1	FC (Index Mark)
26	00 or FF
6*	00
1	FE (ID Address Mark)
1	Track Number
1	00
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	00 or FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	00 or FF
247**	00 or FF

*Write bracketed field 26 times

**Continue writing until FD1781 interrupts out. Approx. 247 bytes.

NON-IBM FORMATS

Non-IBM formats are very similar to the IBM formats except a different algorithum is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II Commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the FD1781, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1781 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

REFERENCES:

1. IBM Diskette OEM Information GA21-9190-1
2. SA900 IBM Compatibility Reference Manual — Shugart Associates.

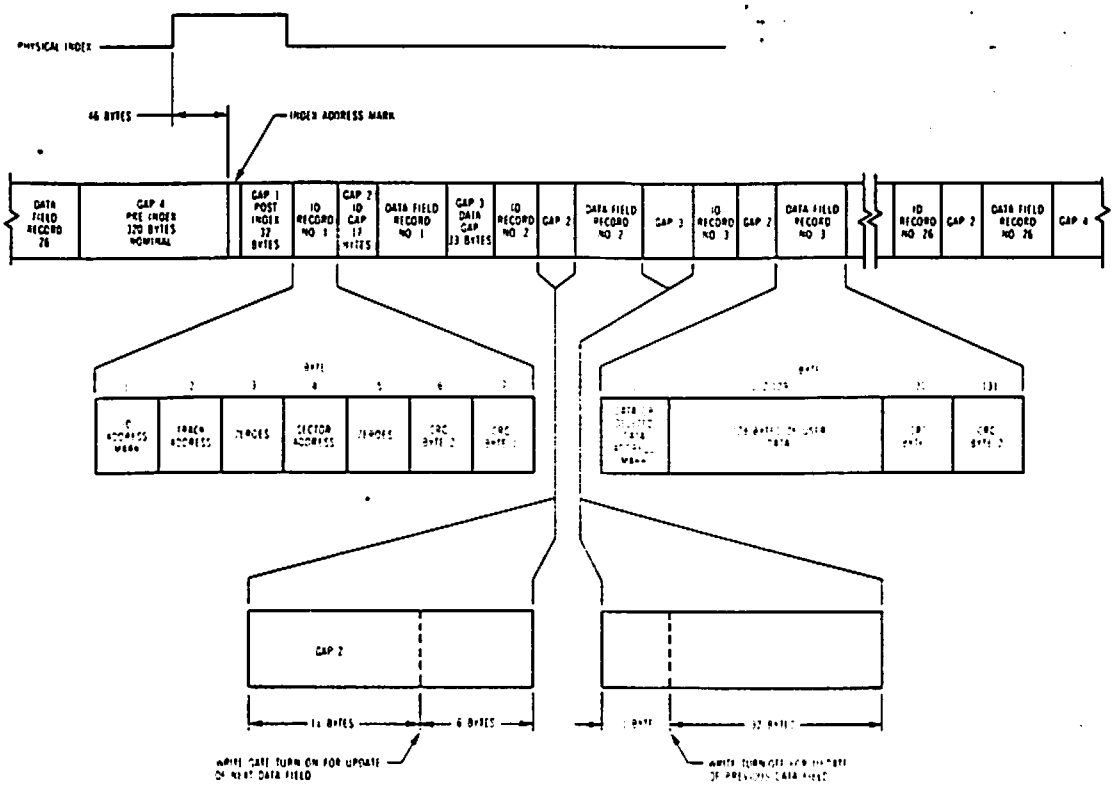

FIG. 13. TRACK FORMAT

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)	+15 to −0.3V
Max. Voltage to Any Input With Respect to V_{SS}	+15 to −0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	−55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ±.6V, V_{SS} = 0V, V_{CC} = +5V ±.25V

V_{DD} = 10 ma Nominal, V_{CC} = 30 ma Nominal

SYMBOL	CHARACTERISTIC	MIN.	TYPE.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	A	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	A	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −100 μA
V_{OL}^*	Output Low Voltage			0.45	V	I_O = 1.6 mA

NOTE: Vol ≤ .4V when interfacing with low Power Schottky parts (1_o < 1 ma)
*except WG, where V_{OL} ≤ .5 volts.

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TIMING CHARACTERISTICS

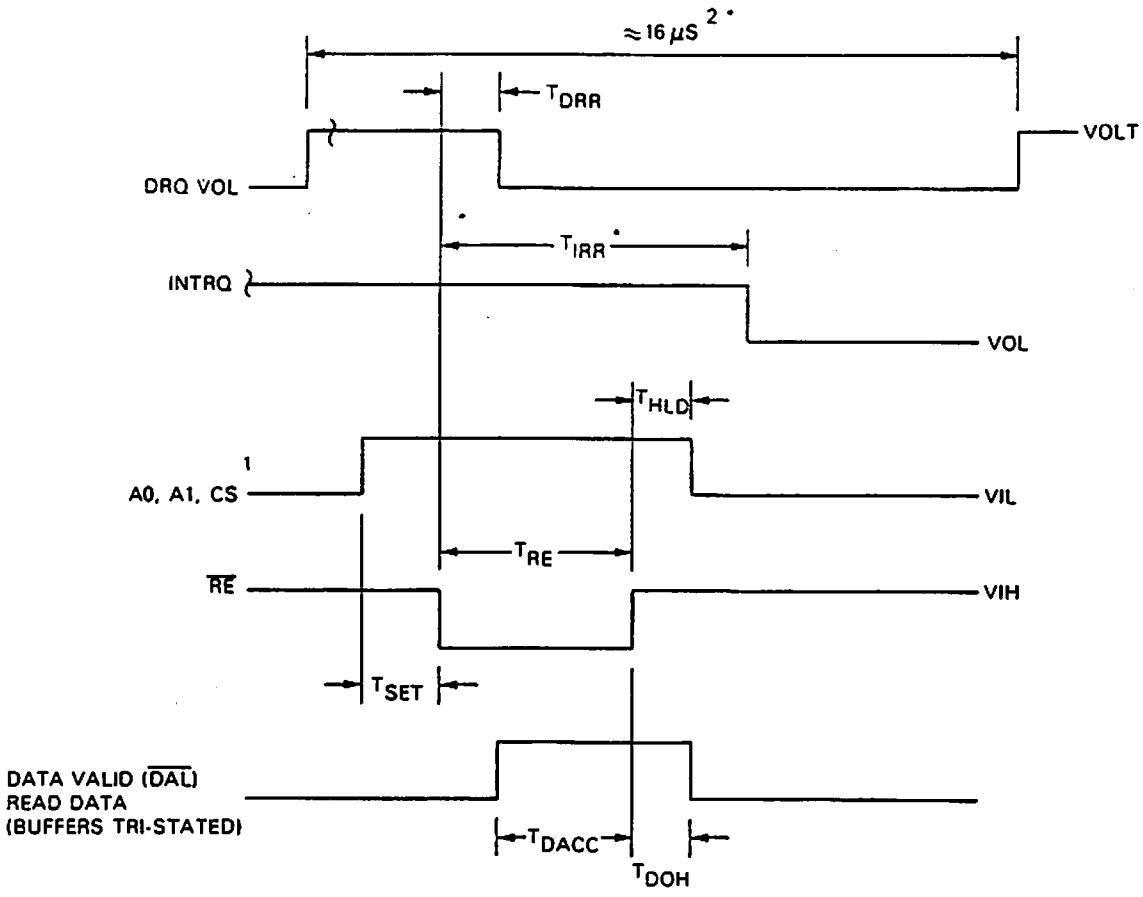
T_A = 0°C to 70°C, V_{DD} = +12V ±.6V, V_{SS} = 0V, V_{CC} = +5 ±.25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

READ OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf

READ ENABLE TIMING



NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. FOR READ TRACK COMMAND. THIS TIME MAY BE 12* TO 32* μSEC WHEN S-0.
*TIME DOUBLES WHEN CLK-1 MHz.

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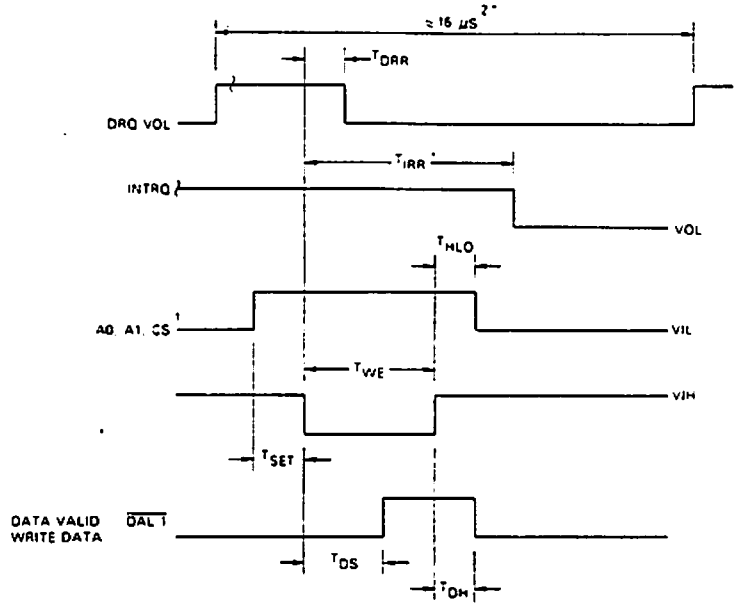
WRITE OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	20			nsec	

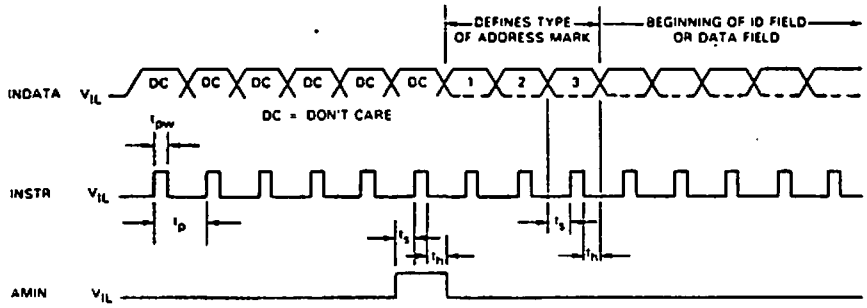
WRITE ENABLE TIMING



NOTE 1 $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
2 WHEN WRITING DATA INTO SECTOR, TRACK OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8 SEC AFTER THE RISING EDGE OF WE WHEN WRITING INTO THE COMMAND REGISTER STATUS IS NOT VALID UNTIL SOME 12 SEC LATER THESE TIMES ARE DOUBLED WHEN CLK 1 MHz

*TIME DOUBLES WHEN CLOCK 1 MHz

INPUT DATA TIMING



t_{pw} 500 ns ± 50 ns
$t_s > 100$ ns
$t_h > 300$ ns
1.2 μs < t_p < 4 ms

NOTE: INSTR MUST BE FREE-RUNNING AS INDICATED BY THE t_p SPECIFICATION. ALSO, THERE MUST BE AT LEAST 2 INSTR PULSES DURING MASTER RESET.

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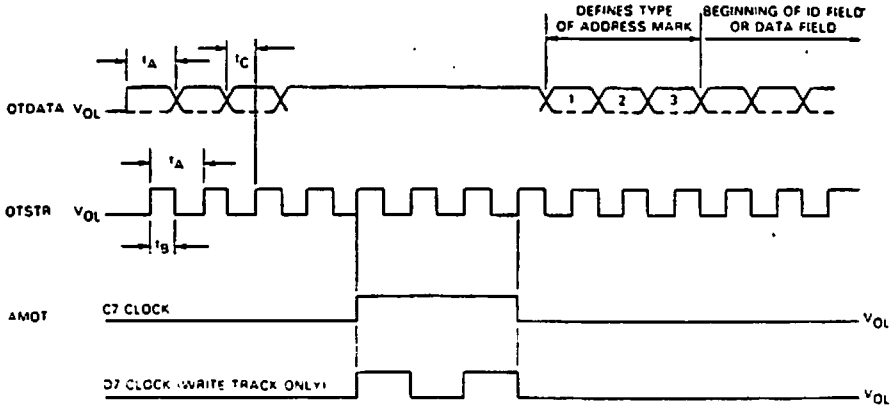
OUTPUT DATA TIMING



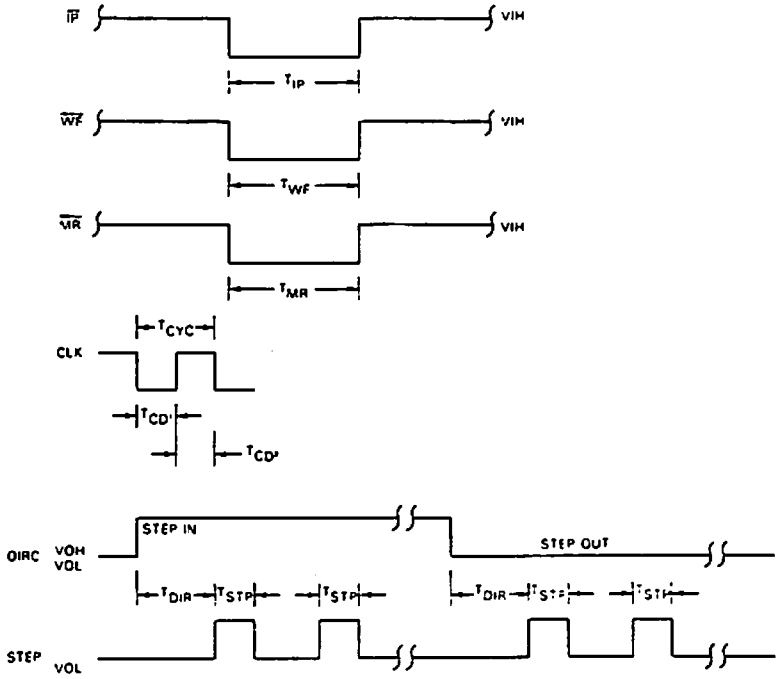
	$\overline{DDEN}$ = 1	$\overline{DDEN}$ = 0
t_A	SEE NOTE	2 µs
t_B		1 µs
t_C		1 µs
		CLK 2 mHz

NOTE:
WHENEVER $\overline{DDEN}$ = 0, OTSTR IS FREE RUNNING AS SHOWN ABOVE
WHEN $\overline{DDEN}$ = 1 & WG = 0 OTSTR IS A SERIES OF FM CLOCK PULSES
WHEN $\overline{DDEN}$ = 1 & WG = 1 OTSTR BECOMES WD AS IN THE FD1771 (i.e. CONTAINS FM CLOCK & DATA PULSES)

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty	175			nsec	2 MHz ±1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	2000			nsec	These times doubled when CLK = 1 MHz
TDIR	Dir Setup to Step	12			µsec	
TMR	Master Reset Pulse Width	5			µsec	
TIP	Index Pulse Width	5			µsec	
TWF	Write Fault Pulse Width	5			µsec	

MISCELLANEOUS TIMING



PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
19	MASTER RESET	$\overline{MR}$	• A logic low on this input resets the device and clears the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive.
COMPUTER INTERFACE:			
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	• Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
3	CHIP SELECT	$\overline{CS}$	• A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0,A1	• These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:
4	READ ENABLE	$\overline{RE}$	• A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	• A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	• This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	• This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	• This input requires a free-running square wave clock for internal timing reference.
FLOPPY DISK INTERFACE:			
25	ADDRESS MARK DETECT IN	AMIN	• Indicates to the FD1781 that an address mark has been detected. The FD1781 assumes the next three data bits defines the type of address mark encountered.
26	INPUT STROBE	INSTR	• Indicates that INDATA is VALID.
27	INPUT DATA	INDATA	The external data recovery circuits present INDATA as an input to the FD1781. INDATA must be valid when INSTR is active, see timing.
31	OUTPUT DATA	OTDATA	• The FD1781 presents output data and is valid when OTSTR is active.

A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	Status Reg	Command Reg
0	1	Track Reg	Track Reg
1	0	Sector Reg	Sector Reg
1	1	Data Reg	Data Reg

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28	HEAD LOAD	HLD	• The HLD output controls the loading of the Read-Write head against the media the HLT input is sampled every 10 nsec. When a logic high is sampled on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	STEP	STEP	• Step and direction motor control. The step output contains a 2 μsec high signal for each step and the direction output is active high when stepping; active low when stepping out.
16	DIRECTION	DIRC	
17	OUTPUT STROBE	OTSTR	• OTSTR when active indicates when the Output data is valid. The leading edge of OTSTR is centered about the data. (See timing) OTSTR becomes Write Data (WD) when DDEN = 1.
18	ADDRESS MARK OUT	AMOT	• AMOT when active informs the external data recovery circuits to write a unique data mark in double density mode. AMOT is valid for three data bits if CLK mark = C7.
29	TRACK GREATER THAN 43	TG43	• This output informs the drive that the Read-Write head is positioned between track 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	• This output is made valid when writing is to be performed on the diskette.
32	READY	READY	• This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	• This input detects writing faults indications from the drive. When WG = 1 and WF goes low the current Write command is terminated and the Write Fault status bit is set. The WF input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	• This input informs the FD1781 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	• Input, when low for a minimum of 10 μsec, informs the FD1781 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	• This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	• This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	• This input is used for testing purposes only and should be tied to +5V or left open by the user.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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4/15/83

ADDENDUM

3650 Series User's Manual

Versions of the 3651 produced after January 1, 1983 incorporate significant design changes which are not reflected in the latest printing of the User's Manual. These changes include the replacement of the delta-gun CRT used in earlier versions with an in-line gun CRT, the addition of automatic degaussing equipment, the elimination of dynamic convergence circuitry (not needed with an in-line tube), and the replacement of the original power supply and CRT deflection circuitry (on the analog circuit board) with newly developed circuitry.

No changes have been made in the logic circuitry, except for that in the keyboard. The new version of the 3651 is operated in the same manner as the earlier versions, except that CPU RESET is a two key operation. The Shift key must be held down while the CPU Reset key is struck to obtain a reset. The display capabilities of the new unit are the same as those of the older unit. Chapters 1 - 14 and Appendices A - G of the User's Manual remain applicable.

Appendix H, concerning alignment, is not applicable to the new version of the 3651. A new alignment procedure is included in this addendum.

In addition, the schematic drawings for the original analog module (101165), convergence module (101162), video module (101174) and keyboard (100878) included in the manual are not applicable. These drawings are superceded by drawing 102350 (new analog module), drawing 101976 (new video module) and drawing 101893 (new keyboard). New units with built-in mini disk drives have a voltage regulator shown on new drawing 102362. An interconnecting wiring diagram is given on drawing 102428. The new drawings are attached to this addendum.

A special **CAUTION** should be observed when installing the modified 3651. The new power supply circuitry includes a line voltage selector switch (SW2) which should be checked for the proper setting before AC power is applied to the terminal. The switch is situated on the analog board and is accessible upon removal of the cabinet cover. The cover is held by two screws situated below the front edge of the keyboard. After these screws are removed, the front of the cover can be lifted straight up. The cover will pivot on a flange at its rear edge until this flange is disengaged from the unit frame. The cover can then be pulled forward and off the unit.

BECKMAN

MMC Horizon™ Systems

FM 761041B-302
April, 1983

CRT Monitor P/N 761258

Operating Instructions

The CRT Monitor displays real-time plots and summary plots from data furnished by the Beckman MMC Horizon System. After setup, the monitor operates automatically. Prompts on the MMC display will permit you to enter variables and scaling information for the real-time plots through the MMC keyboard; after setup, no further manipulation of the CRT keyboard is needed.

After an MMC test has been run, when the MMC is ready to begin printing summary plots, the CRT display will tell you "PRESS SPACE BAR FOR NEXT PLOT." Each time you press the space bar on the CRT keyboard, the next graph in the sequence will be generated. If you wish to cycle rapidly forward, hold down the space bar and the graphs will cycle until you release the space bar.

Set up the CRT Monitor as follows:

a. Locate the Monitor on a table at a convenient viewing height, alongside the MMC.

b. Install the interconnecting cable (P/N 760258) between MODEM receptacle on the Monitor rear panel and the I/O 3 receptacle on the rear panel of the MMC.

c. Insert the power cord into the receptacle marked "120 V, 50/60" on the rear panel of the Monitor.

d. Select a power outlet capable of supplying 120 Vac, 50-60 Hz at 2.5 A. Insert power plug into outlet.

e. The ON-OFF switch is located on the rear panel, at the lower right (as seen when facing the rear panel). Place switch to ON.

f. After a few seconds, the following message will be displayed:

```
DISC BASIC V9.80 COPYRIGHT © 1980
MAXIMUM RAM AVAILABLE?
32049 BYTES FREE
READY
```

g. Should that message not appear, hold down the COMMAND key and press CPU RESET key. This should produce the desired message.

Note

See instructions for the safe handling of diskettes in Part One of the MMC Horizon Systems manual (P/N 761015).

h. Open the door on the disk drive at the right of the screen.

i. Grasp the CRT Plot Program diskette (P/N 760163) with your left thumb over the diskette label.

j. Carefully remove the diskette from its protective paper envelope and insert it into the disk drive with the label facing to the right and the elongated slot away from the operator.

k. Close the disk drive door.

l. Press AUTO key. After a few seconds delay, the screen will display "BECKMAN." The screen will remain unchanged until an MMC test begins. At this time, the display will construct graph axes and begin to plot in real time those variables you have selected in response to MMC prompts.* No operator intervention is required. To review summary plots, see text at the beginning of these instructions.

To shut down Monitor operation:

m. Open disk drive door and remove diskette.

n. Replace diskette in its protective envelope.

o. Place ON-OFF switch to OFF.

To use the CRT Monitor as a separate stand-alone computer, disconnect the MMC interconnecting cable and follow instructions in the "Intecolor User's Manual" (P/N 999276) furnished with the CRT Monitor.

Note

Should color convergence need to be adjusted, instructions are included in the "Intecolor User's Manual" (P/N 999276).

*See Part Two, MMC Horizon System Operating Instructions.

BECKMAN

Beckman Instruments, Inc.
Physiological Measurements Operations
1630 South State College Boulevard
Anaheim, California 92806

ATTENTION!!! ATTENTION!!! ATTENTION!!! ATTENTION!!!

A new keyboard is now being supplied with some Intecolor terminals and microcomputer systems. The new unit has a light grey cover and dark grey alphabetic and numeric keys. Unlike the older keyboard, which has a beige cover, the new unit has no specially colored keys in the main keypad. Check to see if you have the new unit. If you do, follow the important instructions given below. Systems not using the new keyboard are not affected.

The new keyboard is set up at the factory to make CPU RESET a two-key operation.

For reset, hold SHIFT down while CPU RESET is depressed.

This initializes a terminal or microcomputer in the CRT mode. In an FCS microcomputer with BASIC, operation of CPU RESET with the COMMAND key down still initializes the Intecolor in the BASIC mode.

Two-key reset helps avoid unwanted accidental reset. However, the keyboard may be modified quite easily for one-key reset if this is desired. Simply remove the PCB assembly from its enclosure and install a jumper at location W2. In either configuration for reset a logic low is applied to edge connector terminal 26.

In the User's Manual, disregard references to the colors of certain alphabetic and numeric keys in the main pad. On the new keyboard these keys are not specially color coded. In addition, note that the keys in the small pad on the left of the unit have colored dots rather than being completely colored.

Press Auto after CPU Ready to Installing Demo or Plot

FORMATTER

This program enables the user to format blank 5 inch mini-floppy* diskettes for use with the Compucolor II.

INSTRUCTIONS:

Load the formatter program by inserting the diskette and hitting the "AUTO" key. Remove the formatter immediately to avoid accidently formatting it

After the program has loaded the following will be displayed:

```
COMPUCOLOR DISKETTE FORMATTER
FORMAT OR READ CHECK?>
```

If "F" is entered the program will format a disk. Entering "R" performs a read check on a previously formatted diskette. The read check will not destroy any information on the disk. Formatting a diskette will destroy ALL previous data. If you wish to return to BASIC, type "E".

After "F" or "R" is entered the program will display:

```
DRIVE NUMBER?>
```

Enter "0" to format and/or read check a disk on the internal drive or "1" for an external drive. The format/read check will begin immediately after "0" or "1" is hit.

A read check is always performed regardless of the option selected. Any errors detected are displayed according to the following format:

```
T01S01 or T26S08
```

The numbers following "T" and "S" indicate the respective track and sector (in hex) where an error occurred. There are many kinds of errors and it is impossible for the user to determine which type occurred. Although the system can tolerate some errors it is recommended that the user re-format a diskette if any errors occur. Once a disk has been successfully formatted it can be initialized and used for programming and file storage in the Compucolor II.

*The Compucolor II does not use the optical hole placed on diskettes. Therefore either soft or hard-sectored diskettes may be used.

Instructions for Formatting and Initializing Blank Discs for Use with the ISC 3560 Computer

1. Turn on computer power. If already on, type ESCape-W-Return.
2. Insert ISC Formatter disc in disc drive.
3. Press AUTO KEY.
4. Select option 1 (single sided 5¼ inch MD discs) and press RETURN.
5. Type F (for format) in response to Format or Read Check prompt.
6. Remove the formatter disc from the disc drive. Insert the blank disc to be formatted.

   ****WARNING**** Failure to remove the formatter disc before this next step will result in the formatter disc itself being formatted, thus erasing the program on it and rendering it useless for future formatting!

7. Type Ø in response to Disc Drive prompt.

   The blank disc in the disc drive will now be formatted. The process takes about two minutes.

8. The disc is not yet ready for use. It needs to be initialized (given a volume name) first. The procedure is as follows:

   a. Press shift and CPU reset at the same time.

   b. Press ESCape-D. The prompt FCS> should appear. This is the File Control System operating system prompt.

   c. With the previously formatted disc still in the disc drive, type the following command:

      INI MDØ: <volume name> and Return where <volume name> is a word up to eleven characters with no spaces or punctuation. This becomes the disc's volume name.

9. The disc is now ready for storage of programs or data files using the SAVE command (see the ISC Intecolor user's manual).

MMC HORIZON CRT

Early model MMC Horizons (shipped prior to Dec. 1984) were sold with the optional Intelegent Systems CRT (ISC). This portable desktop computer was used to provide real time and summary report plots.

The CRTs were shipped with a power cord, interface cable 760258, Formater Diskette, and Sampler Program Diskette. To operate the CRT with the MMC Horizon the operator utilized a special CRT Plot Program Disk in the CRT disk drive. The part number for one of these disks is 760163.

CRT operating instructions are enclosed for both the ISC CRT and the Texas Instruments CRT.

FORMATTER

This program enables the user to format blank 5 inch mini-floppy* diskettes for use with the Compucolor II.

INSTRUCTIONS:

Load the formatter program by inserting the diskette and hitting the "AUTO" key. Remove the formatter immediately to avoid accidently formatting it.

After the program has loaded the following will be displayed:

```
COMPUCOLOR DISKETTE FORMATTER
FORMAT OR READ CHECK?>
```

If "F" is entered the program will format a disk. Entering "R" performs a read check on a previously formatted diskette. The read check will not destroy any information on the disk. Formatting a diskette will destroy ALL previous data. If you wish to return to BASIC, type "E".

After "F" or "R" is entered the program will display:

```
DRIVE NUMBER?>
```

Enter "0" to format and/or read check a disk on the internal drive or "1" for an external drive. The format/read check will begin immediately after "0" or "1" is hit.

A read check is always performed regardless of the option selected. Any errors detected are displayed according to the following format:

```
T01S01 or T26S08
```

The numbers following "T" and "S" indicate the respective track and sector (in hex) where an error occurred. There are many kinds of errors and it is impossible for the user to determine which type occurred. Although the system can tolerate some errors it is recommended that the user re-format a diskette if any errors occur. Once a disk has been successfully formatted it can be initialized and used for programming and file storage in the Compucolor II.

*The Compucolor II does not use the optical hole placed on diskettes. Therefore either soft or hard-sectored diskettes may be used.

ATTENTION!!! ATTENTION!!! ATTENTION!!! ATTENTION!!!

A new keyboard is now being supplied with some Intecolor terminals and microcomputer systems. The new unit has a light grey cover and dark grey alphabetic and numeric keys. Unlike the older keyboard, which has a beige cover, the new unit has no specially colored keys in the main keypad. Check to see if you have the new unit. If you do, follow the important instructions given below. Systems not using the new keyboard are not affected.

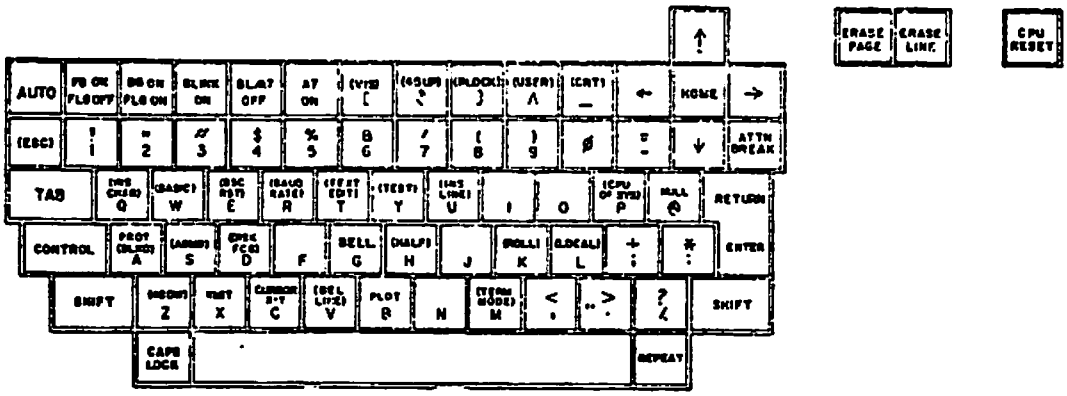
The new keyboard is set up at the factory to make CPU RESET a two-key operation.

For reset, hold **SHIFT** down while **CPU RESET** is depressed.

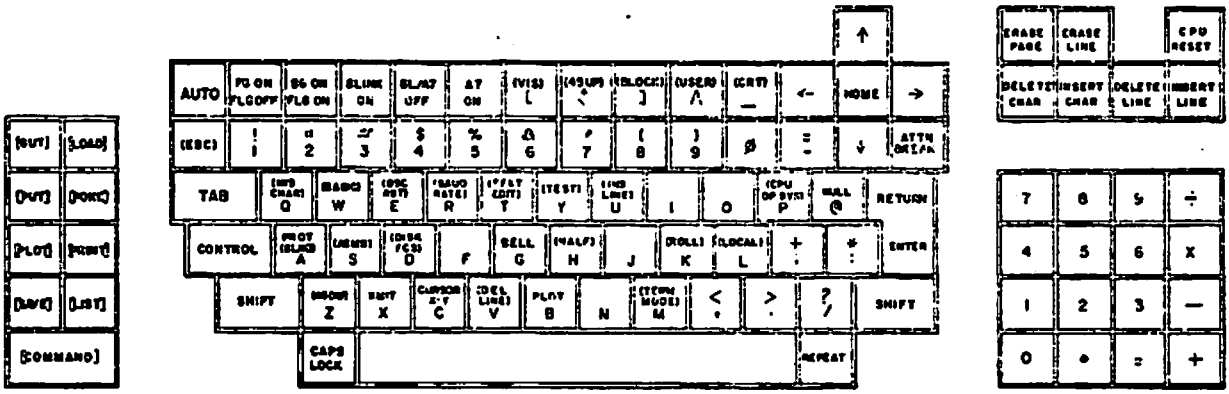
This initializes a terminal or microcomputer in the CRT mode. In an FCS microcomputer with BASIC, operation of CPU RESET with the COMMAND key down still initializes the Intecolor in the BASIC mode.

Two-key reset helps avoid unwanted accidental reset. However, the keyboard may be modified quite easily for one-key reset if this is desired. Simply remove the PCB assembly from its enclosure and install a jumper at location W2. In either configuration for reset a logic low is applied to edge connector terminal 26.

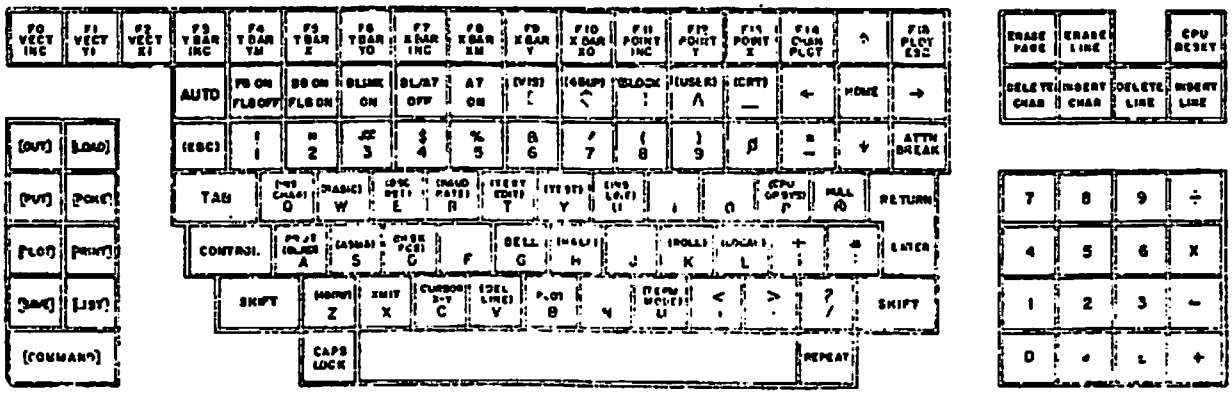
In the User's Manual, disregard references to the colors of certain alphabetic and numeric keys in the main pad. On the new keyboard these keys are not specially color coded. In addition, note that the keys in the small pad on the left of the unit have colored dots rather than being completely colored.



72 - KEY



101 - KEY



117 - KEY

BECKMAN

MMC Horizon™ Systems

FM 761041-301
March, 1983

CRT Monitor P/N 760393

Operating Instructions

The CRT Monitor displays real-time plots and summary plots from data furnished by the Beckman MMC Horizon System. After setup, the monitor operates automatically. Prompts on the MMC display will permit you to enter variables and scaling information for the real-time plots through the MMC keyboard; after setup, no further manipulation of the CRT keyboard is needed.

After an MMC test has been run, when the MMC is ready to begin printing summary plots, the CRT display will tell you "PRESS SPACE BAR FOR NEXT PLOT." Each time you press the space bar on the CRT keyboard, the next graph in the sequence will be generated. If you wish to cycle rapidly forward, hold down the space bar and the graphs will cycle until you release the space bar.

Set up the CRT Monitor as follows:

a. Locate the Monitor on a table at a convenient viewing height, alongside the MMC.

b. Install the interconnecting cable (P/N 760258) between MODEM receptacle on the Monitor rear panel and the I/O 3 receptacle on the rear panel of the MMC.

c. Insert the power cord into the receptacle marked "120 V, 50/60" on the rear panel of the Monitor.

d. Select a power outlet capable of supplying 120 Vac, 50-60 Hz at 2.5 A. Insert power plug into outlet.

e. The ON-OFF switch is located on the rear panel, at the lower right (as seen when facing the rear panel). Place switch to ON.

f. After a few seconds, the following message will be displayed:

```
DISC BASIC V9.80 COPYRIGHT © 1980
MAXIMUM RAM AVAILABLE?
32049 BYTES FREE
READY
```

g. Should that message not appear, hold down the COMMAND key and press CPU RESET key. This should produce the desired message.

Note

See instructions for the safe handling of diskettes in Part One of the MMC Horizon Systems manual (P/N 761015).

h. Open the door on the disk drive at the right of the screen.

i. Grasp the CRT Plot Program diskette (P/N 760163) with your left thumb over the diskette label.

j. Carefully remove the diskette from its protective paper envelope and insert it into the disk drive with the label facing to the right and the elongated slot away from the operator.

k. Close the disk drive door.

l. Press AUTO key. After a few seconds delay, the screen will display "BECKMAN." The screen will remain unchanged until an MMC test begins. At this time, the display will construct graph axes and begin to plot in real time those variables you have selected in response to MMC prompts.* No operator intervention is required. To review summary plots, see text at the beginning of these instructions.

To shut down Monitor operation:

m. Open disk drive door and remove diskette.

n. Replace diskette in its protective envelope.

o. Place ON-OFF switch to OFF.

To use the CRT Monitor as a separate stand-alone computer, disconnect the MMC interconnecting cable and follow instructions in the "Intecolor User's Manual" (P/N 999276) furnished with the CRT Monitor.

Note

Should color convergence need to be adjusted, instructions are included in the "Intecolor User's Manual" (P/N 999276).

*See Part Two, MMC Horizon System Operating Instructions.

BECKMAN

Beckman Instruments, Inc.
Physiological Measurements Operations
1630 South State College Boulevard
Anaheim, California 92806

PM83026-383-.25V

Printed in USA

Intecolor
AN INTELLIGENT SYSTEMS COMPANY

8000/8300 PARTS REPLACEMENT CONTRACT

OPTION 60

The Parts Replacement Contract provides a one-year warranty on all assemblies and peripherals manufactured by Intecolor Corporation. Unit or card sub-assembly replacements will be shipped from the factory within 24 hours. If you purchase the Parts Replacement Contract, Option 60, on your initial order, the cost is 12% per unit, minimum of $300. If Option 60 is purchased after the unit has been shipped, but within 90 days, the cost is 15% per unit, minimum of $350. The Parts Replacement Contract may also be purchased after the warranty period — the unit must be 100% functional at the time the contract is purchased. Pricing will be quoted from the factory.

NOTE: The purchase price of a Parts Replacement Contract is non-refundable. Subsequent renewals are the customer's responsibility and must be purchased before the existing Parts Replacement Contract expires.

Upon notification of a problem, Intecolor will attempt to diagnose the problem, suggest a solution over the phone, and agree to a course of action to get the unit operational as soon as possible. Subassemblies that are required to correct the problem will be shipped within 24 hours of the customer's contact. This type turn-around should result in a 48-hour maximum down-time. If the source of the problem cannot be found, a replacement of the entire subsystem will be made. Under a Parts Replacement Contract, shipping charges are paid one way by the customer and one way by Intecolor. All items must be shipped prepaid.

Contract Period: From _____ To _____

Intecolor Corporation
Authorized Signature:

Signed _____

By _____

Title _____

Date _____

Customer:

Company _____

Address _____

_____

Customer's Authorized Signature:

Signed _____

Please Print Name _____

Title _____

Phone _____

Date _____

[illegible] 404/449-5961

H. ALIGNMENT

Like other equipment made at Intelligent Systems Corporation, the 3651 is thoroughly tested and aligned at the factory before it is shipped. It generally requires complete realignment only after extensive repairs have been made. However, there are several routinely encountered situations which call for minor adjustments. Among them are the following:

1) Upon initial installation of the terminal, after its movement from one place to another, or after physical changes have been made in the area where it is used, irregularities in performance are observed which are attributable to a misalignment of controls resulting from shocks received by the unit during transportation or to the effects of changed environmental conditions.

2) After an extended period of use, minor performance irregularities are noted which can be attributed to the effects of component aging.

3) After the repair, replacement or modification of the logic board, performance irregularities are noted which can be attributed to the effects of a low supply voltage to the logic circuits due to increased loading of the 5V supply.

The instructions given in this section of the manual are arranged to facilitate both a complete realignment and a quick touch-up of the controls. The complete alignment procedure is described beginning on the following page, while all the instructions pertinent to a touch-up are designated by asterisks.

IMPORTANT NOTE: Whenever a terminal is to be adjusted, whether before being put in service for the first time, or after a period of service, it is good practice to make the following checks before AC power is applied:

a) Remove the cabinet cover and make sure that the line voltage selector switch, SW2, is properly set for either 115V or 220V (single phase only). The cover is held by two screws at the front edge of the unit below the keyboard.

b) Verify that the proper fuse (1.5A, 250V, "Slo-Blo" for 115V or .75A, 250V "Slo-Blo" for 220V) is installed in the line fuse holder on the rear panel of the analog board.

Tools and Equipment Needed

Plastic alignment tool (universal type)

Multirange DC voltmeter (20K ohms/V or better, digital recommended)

High voltage probe for meter

Oscilloscope (DC to 15 MHz)

0-1 DC milliammeter, insulated for 35KV (optional, for adjustment of CRT beam current)

Preliminary Considerations

A complete alignment of the 3651 terminal begins with checks and adjustment of the low voltage power supplies on the analog board. These initial steps are taken with the horizontal and vertical deflection coils, video, logic and high voltage circuits disconnected. Disconnection prevents damage to these components due to improper supply voltages.

In some cases, the analog board will have been removed from the cabinet to facilitate repairs. It may be left out of the cabinet during the tests described below in steps 1 - 6, provided that a sheet of cardboard or other suitable material is placed under it to insulate it from the work table. Subsequent steps require that it be installed in the cabinet, unless the interconnecting cables are replaced with extended cables, which can be made up in the shop.

When no repair work has been done and only a touch-up of the controls is needed, it is not necessary to remove the board, since all the controls are accessible upon removal of the cabinet cover. The cover is held by two screws at the front edge of the unit below the keyboard. The three screws along the top rear edge of the unit hold the cabinet's rear panel and need not be removed.

WARNING: Under no circumstances should the boards be replaced in the cabinet and allowed to rest on the rails at the sides of the cabinet frame or on the inner surfaces of the cabinet while power is on. Short circuits and/or the appearance of dangerous voltages on the frame could result. (The inside surfaces of the unit's plastic base pan and cover are sprayed with a conductive paint.)

Low Voltage Power Circuitry

1) Before applying AC power to the analog board, make certain that the cables terminating at J10 (logic board power), J11 (sync), J6 (vertical deflection coil), J7 (horizontal deflection coil and high voltage interlock), and J8 (video board power) are disconnected. In addition, the black wires to the CRT ground strapping, the CRT anode lead, the brightness control cable (terminating at J9), the degaussing coil leads (terminating at J2), and the fan leads (terminating at J13) may be disconnected. **Double-check the position of SW2, the line voltage selector switch.**

2) Set R13 (5V ADJ) and R19 (PWR FREQ) to their mid-range positions.

** 3) R22 (OVERCURRENT) should be turned full clockwise. In this position maximum sensitivity of the protection circuit is attained.

4) After applying power, use an accurate DC voltmeter to verify the presence of

+12V, +/- .5V, at pin 1 J10 (GND is pins 7 and 8)
-12V, +/- .5V, at pin 2 J10
- 5V, +/- .5V, at pin 6 J10

5) With a DC voltmeter, check for +70V, +/- 5V, (in reference to chassis ground) at the ungrounded end of R9.

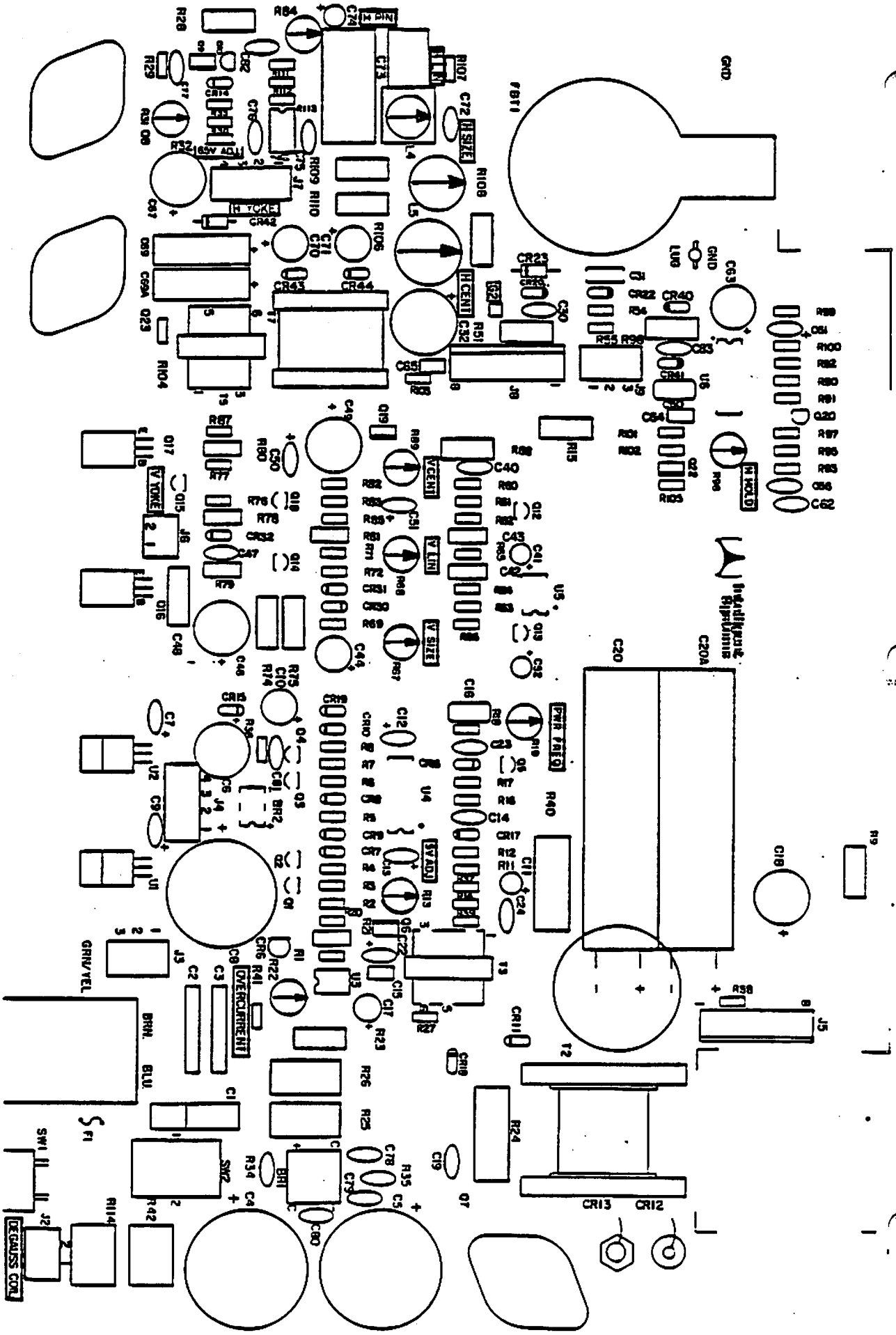
** 6) With a DC voltmeter, check for +5.1V at pins 4 and 5, J10 (pins 7 and 8 are ground). Adjust R13 (5V ADJ) for exactly 5.1V.

NOTE: The power supply frequency control, R19, must be adjusted later, after the horizontal and high voltage circuitry has been adjusted.

7) Remove AC power.

8) Make the appropriate connections of the cables terminating at J2, J10, J11, J13, J6, J7, J8 and J9 on the analog board. The CRT anode lead and the black wire from the CRT ground strapping to the analog board must also be connected. These connections activate the horizontal, vertical high voltage, logic and video circuits and the degaussing coil.

WARNING: J5 and J12 on the analog board are not used when this board is installed in the 3601 terminal. Care must be taken to avoid installing any cable at these points, since damage to circuitry could result.


H SIZE
H CENT
H HOLD
H LIN
H YOKE
V CENT
V LIN
V SIZE
V YOKE
5V ADJ
PWR FREQ
OVERCURRENT
DEGAUSS COIL
GRN/YEL
BRN
BLU
R01966 IP4

9) If there is reason to believe that substantial misadjustment of any or all of the controls has occurred, they should be set initially as follows:

R31	High Voltage Adj.	Mid-range
—	Focus	Mid-range
—	Screen (CRT G2)	See step 15
R115	Brightness	Full CW
R1	Red Cathode	Full CW
R3	Green Cathode	Full CW
R5	Blue Cathode	Full CW
R96	Hor. Freq. (Hold)	3/4 CW
R106	Hor. Centering	Mid-range
L4	Hor. Linearity	Arbitrary
L5	Hor. Size	Slug in
R67	Vert. Size	Mid-range
R68	Vert. Linearity	Mid-range
R89	Vert. Centering	Mid-range
R84	Pincushion	Full CCW

High Voltage Circuitry

** 10) With AC power removed, connect a reliable DC voltmeter with high voltage probe to the unit. This is done by first fixing the ground clip of the probe to a suitable point on the chassis and then slipping the tip of the probe under the anode cap of the CRT, making certain that a good connection is maintained.

** NOTE: All instructions for giving keyboard commands suppose that the terminal is operating in the Local mode. The terminal is automatically placed in this operating mode at power up unless a special feature has been installed. After power is applied, the terminal can be placed in the Local mode at any time by operating the CPU Reset key with holding down the Shift key.

** 11) After applying AC power, use the following sequence of keyboard operations to obtain a black screen (The cursor will remain visible in the upper left corner.)

"Shift" and "CPU Reset", "Erase Page"

A black screen is coincident with minimum CRT beam current, at which the high voltage should be set.

** 12) Adjust R31 for a reading of 25KV on the meter.

NOTE ON X-RADIATION: At an anode voltage of 25KV, X-ray emissions from the CRT will average about .05 mRh/hr. Factory tests of the tube at 30KV and higher indicate a radiation level of .18 mRh/hr maximum. Thus, throughout the range of adjustment of the high voltage supply, levels are well below the .5 mRh/hr maximum prescribed by the Dept. of HEW. Nevertheless, it is recommended that the tube not be operated at higher anode voltages.

** 13) A check of the high voltage circuitry under maximum loading is made after obtaining a white screen with the following keyboard operations:

"BG ON FLG ON", "Control" together with "W (white)", "Erase Page"

The anode voltage indicated by the meter should drop to around 24.2KV.

** 14) Adjustment of the focus control is facilitated by placing a pattern of white dots over a black background on the screen. The sequence of keyboard operations given at the top of the next page causes this display to appear:

"Shift" and "CPU Reset", "Erase Page", "ESC", "Y", "."

The focus control (adjacent to the flyback transformer on the side of the analog board) is adjusted to maximize the sharpness of the dot pattern.

15) The CRT control grid (G2) bias affects the overall beam current of the tube. It is adjusted with the control labeled "screen", which is situated immediately below the focus control. There are two possible methods of adjustment. The one to be described first is that used at the factory, which requires special equipment. The second method is suggested when this equipment is not available.

a) At the factory, the control is set to give a CRT beam current of 500 microamps with a white screen and the brightness control full clockwise. A specially insulated DC milliammeter is inserted in the CRT anode lead to indicate the beam current. After adjustment this control is locked in place. It should not require readjustment unless components in the high voltage circuitry or the CRT itself are replaced.

b) If it is necessary to readjust this control and a properly insulated meter is not available; it should be set initially at a point about 1/8 turn in the clockwise direction from full counter-clockwise. If this setting is too low it will not be possible to obtain sufficient brightness with the brightness control. If it is too high, a phenomenon known as overscan, in which a raster ghost will appear when the screen should be black, will be seen. This may be checked by switching from a white screen to a black screen with the brightness control all the way up and by trying to completely darken the screen with the brightness control while a white raster is present. Prolonged operation of the unit with the control set excessively high will overload the power supplies, activating the overcurrent protection circuit.

Horizontal and Vertical Deflection Circuitry

** 16) The horizontal oscillator frequency can be adjusted in either of two ways. With both methods the aim is to make the oscillator frequency somewhat lower than the frequency of the synchronizing signal from the logic circuitry.

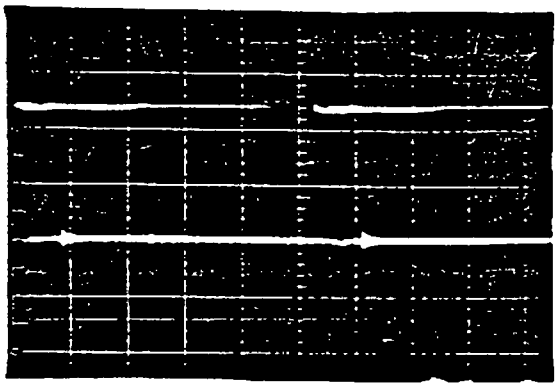
a) A DC voltmeter can be used to monitor the voltage at pin 9 of U6 while R96, the horizontal frequency or "hold" control, is adjusted for a reading of +6V to +6.5V.

b) The alternative is to adjust R96 while monitoring the waveform of the signal at pin 2 of U6 with an oscilloscope. On an oscilloscope, the signal will appear as shown in one of the photographs at the top of the next page. Turn R96 counter-clockwise, if necessary, to obtain a signal similar to the one at left. Turn R96 clockwise until the edges of the signal appear sharply defined, as in the photograph at the right. Continue turning the control clockwise another 30 degrees.

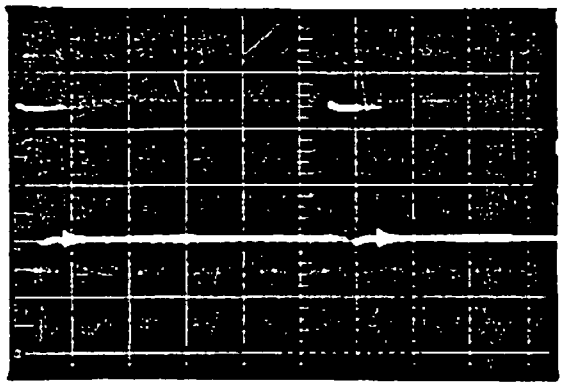
Oscilloscope

Sync - Int Coupling - DC
Sweep - 10 microsec/div Vert - 10 V/div

Oscillator out of sync



Oscillator in sync



17) Using an oscilloscope, measure the DC voltage at the collector of Q16 (tied to R74). It should be about +45V.

Oscilloscope

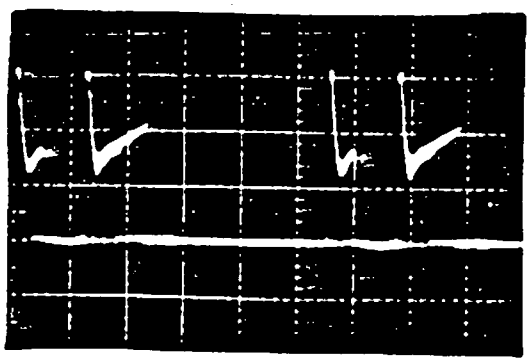
Sync - Int
Sweep - Arbitrary
Coupling - DC
Vert - 10 V/div

** 18) The power frequency control, R19, should now be adjusted to bring the power supply oscillator into sync with the horizontal oscillator. The aim of the adjustment is to make the power supply frequency somewhat lower than that of the horizontal oscillator. Place an oscilloscope probe on the collector (tab) of Q6 and monitor the signal. With the oscilloscope in sync, it will appear either as a series of overlapping waves, as illustrated in the photograph on the left below, or as a single well defined wave, as shown in the photograph on the right. Turn R19 clockwise, if necessary, to obtain the waveform shown in the photograph on the left. Then turn the control counter-clockwise until the waveform shown in the photograph on the right is obtained. Continue turning the control counter-clockwise another 30 degrees.

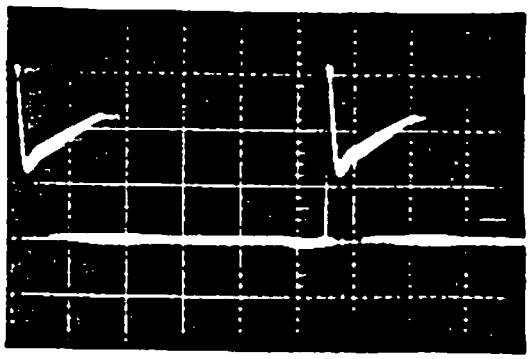
Oscilloscope

Sync - Int
Coupling - DC
Sweep - 10 microsec/div
Vert- 5 V/div

Oscillator out of sync



Oscillator in sync



** 19) Obtain a green raster by the following keyboard operations:

"BG ON FLG ON", "Control" together with "R" (green), "Erase Page"

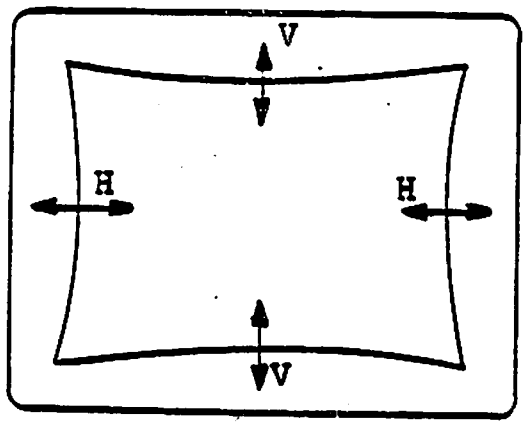
** 20) Adjust R67, the vertical size control, for a raster height of 7.25 inches.

** 21) Center the raster on the vertical axis by adjusting R89.

** 22) Adjust L5, the horizontal size control, for a raster width of 9.5 inches.

** 23) Center the raster on the horizontal axis by adjusting R106.

** 24) Adjust the pincushion control, R84,to obtain a raster with straight sides. The effects of this adjustment are illustrated in the drawing below.



** 25) Obtain a white raster using the following sequence of keyboard operations:

"BG ON FLG ON", "Control" together with "W" (white), "Erase Page"

Readjust R13 for exactly +5.1V, measured at pin 4 or 5, J10.

** 26) After changing the screen from green to black readjust the high voltage. For details, refer to steps 13, 14 and 15.

** 27) Obtain a display of green horizontal lines on a black background with the following sequence of keyboard operations:

"Erase Page", "BG ON FLG ON", "Control" together with "P" (black), "FG ON FLG OFF", "Control" together with "R" (green), "ESC", "Y", "_" (underline)

Adjust R68, the vertical linearity control, for equal spacing of the lines.

Erase the screen with the "Erase Page" key.

** 28) With the following sequence of commands, obtain a green diagonal line on a black background:

"Control" together with "B", "Control" together with "Shift" and "Null", "Control" together with "Shift" and "Null", "Control" together with "2", "Shift" together with "_", "Shift" together with "_", "Control" together with "Shift" and "?"

Adjust L4, the horizontal linearity control, for the straightest possible line. Note that the control has a cam action. The full range of adjustment is covered in a single revolution, and continued turning of the control in either direction results in the repeated traversing of the range.

** **NOTE:** Because of interaction of the vertical, horizontal and high voltage controls, it may be necessary to repeat the adjustments in order to obtain the best results.

Video Circuitry

** 29) The gain controls for the video amplifiers, R1 (red), R3 (green) and R5 (blue), situated on top of the small board at the base of the CRT, may be adjusted by the following method:

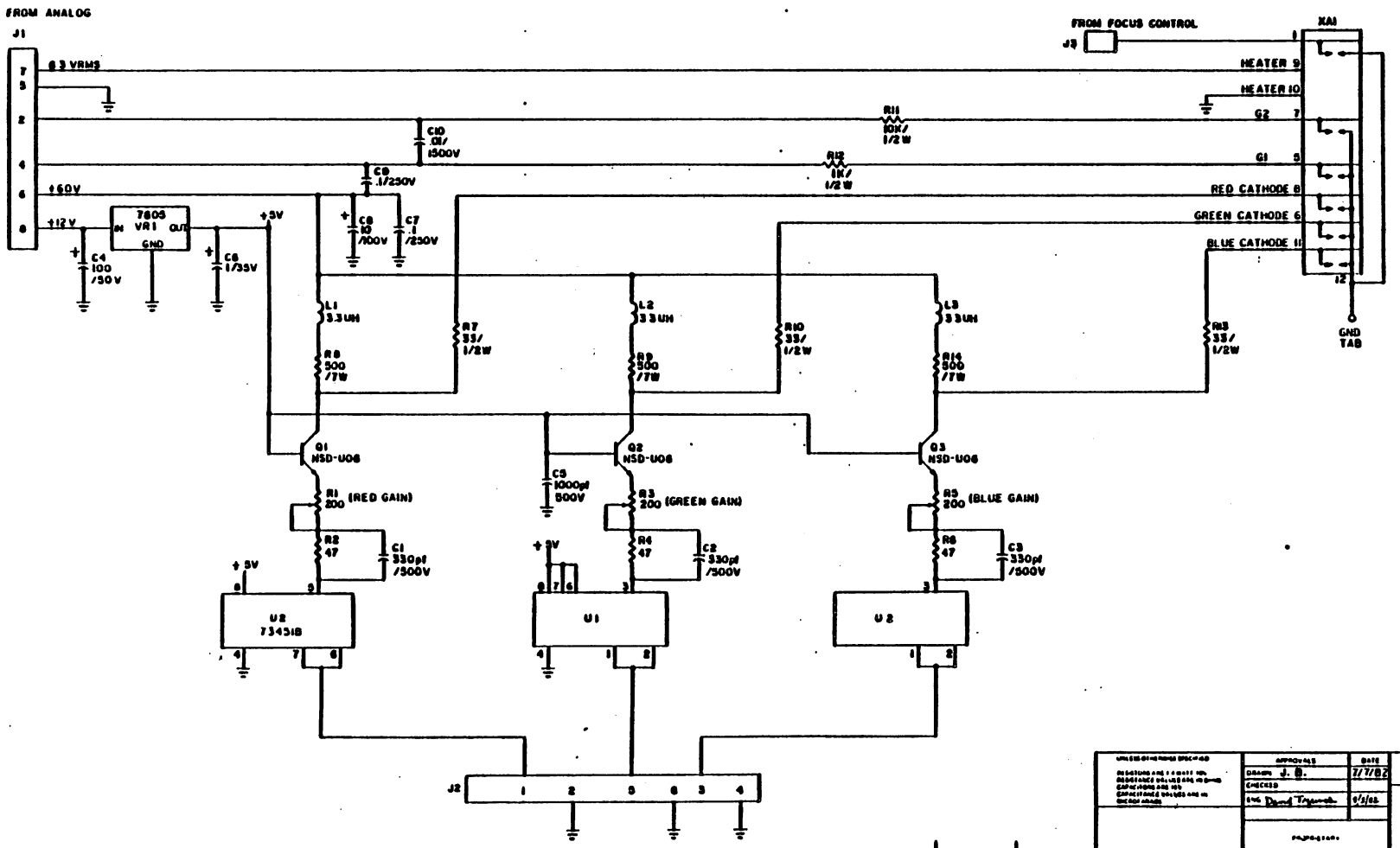
Obtain a white screen by the keyboard commands "BG ON FLG ON", "W" (white), "Erase Page"

Dim the screen with the brightness control, R115. With the control set about 3/4 of full clockwise the raster should remain visible and be of about the right intensity for the gain adjustments.

Set R3 (green) about 15 to 20 degrees from full clockwise. Bring R1 (red) and R5 (blue) down in turn from full clockwise to the points at which the screen is whitest. R1 should be set so that the screen is neither too blue nor too red. R5 should be set so that it is neither too blue nor too yellow.

After setting all three gain controls, turn up the brightness. There should be no loss of whiteness.

A final check is made by obtaining a raster in each of the colors in turn. Use the command sequence "BG ON FLG ON", "(color key)", "Erase Page" to obtain the rasters. Each color should be pure and distinct.



REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG RELEASE	2782	02-02	DAT

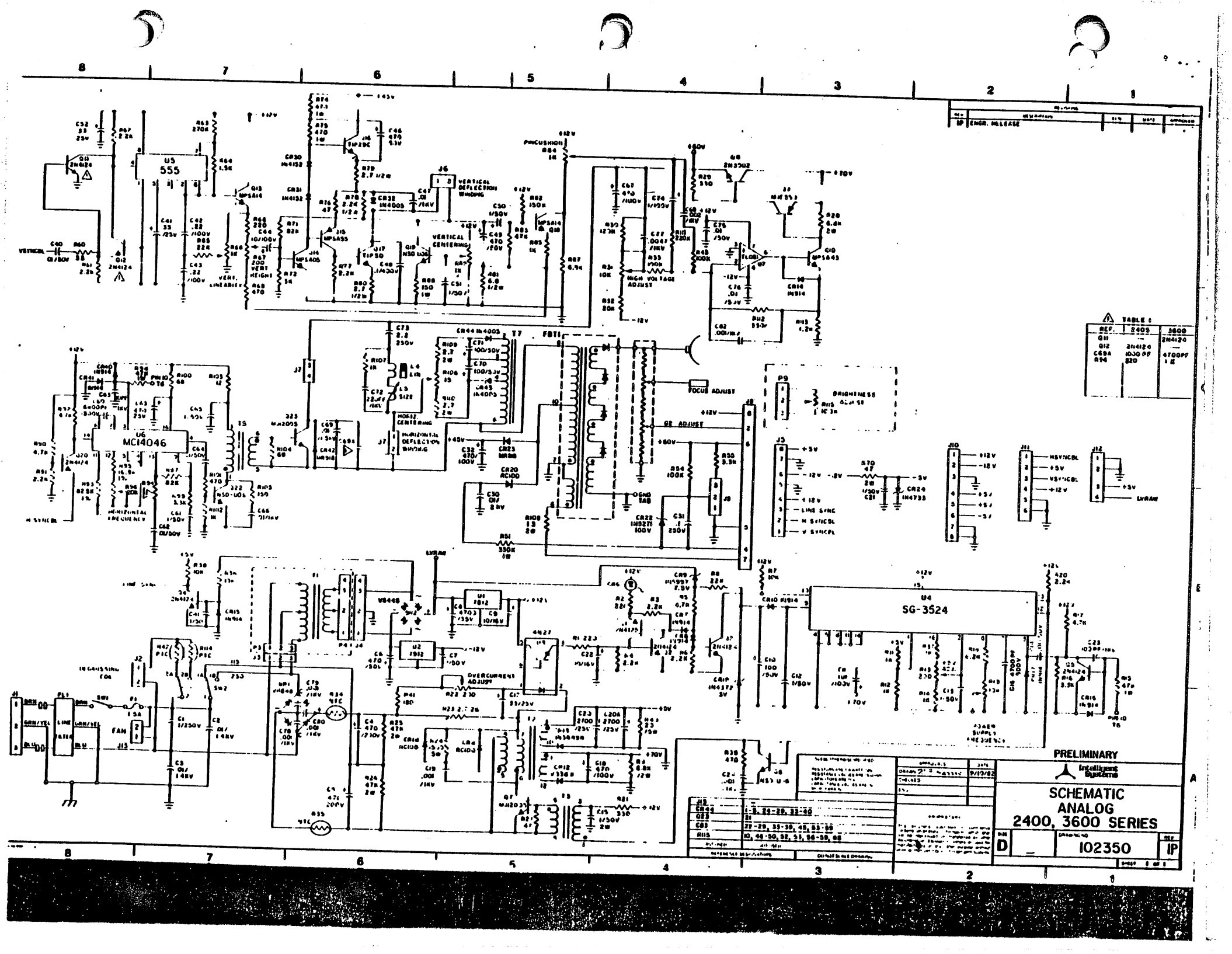
DRAWN	J. B.	7/7/82
CHECKED		
ENG	David Tripoli	9/1/82

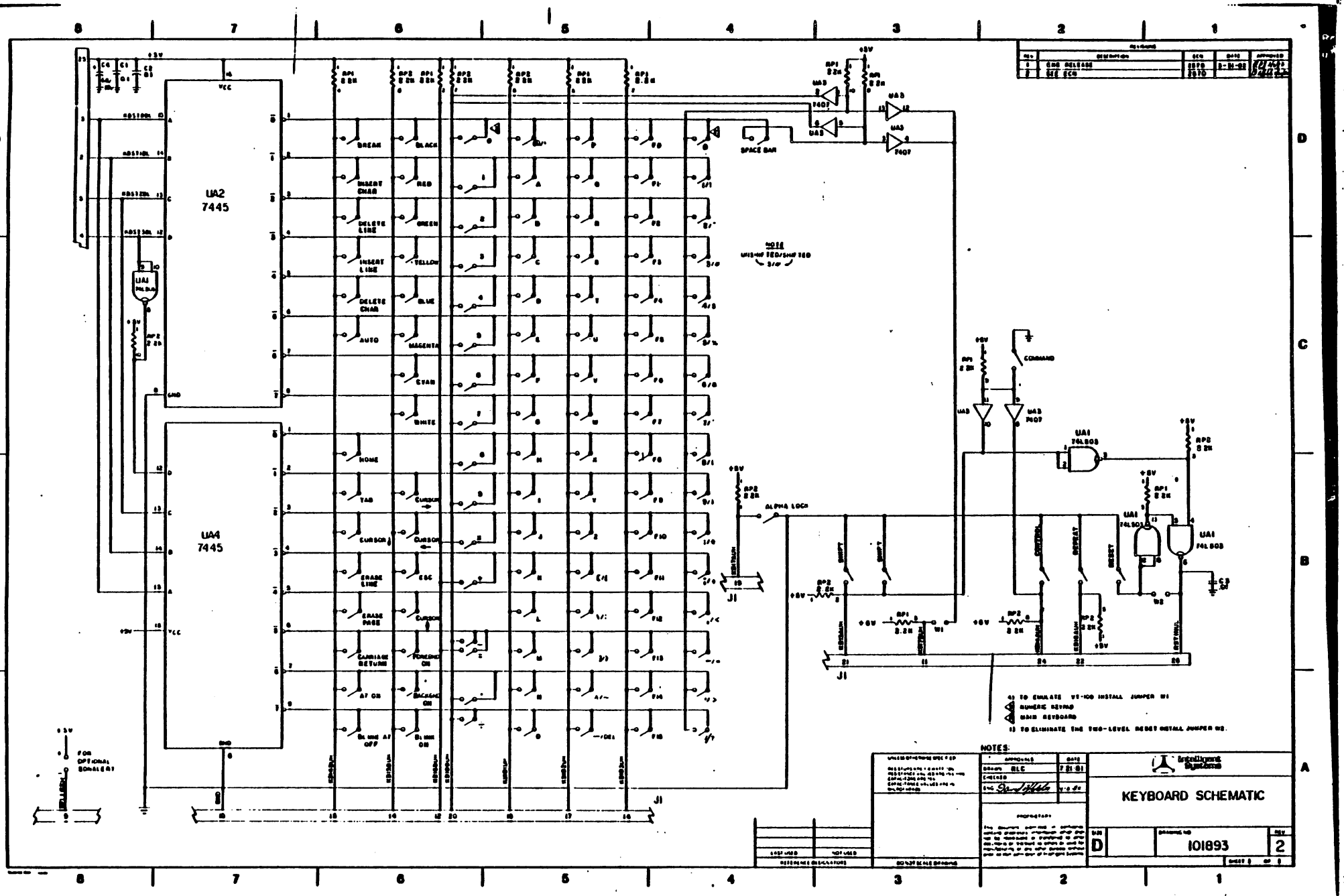
Intelligent Systems

SCHEMATIC
LCCT VIDEO
2400 SERIES

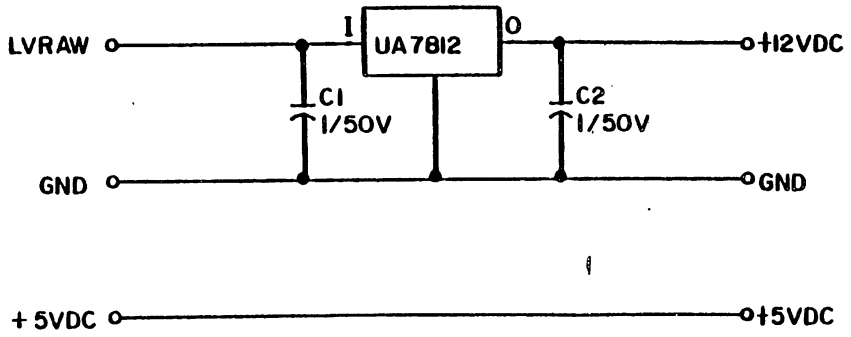
SIZE D | DRAWING NO. 101976 | REV 1

SHEET 1 OF 1


U5
555
U6
MC14046
U4
SG-3524
PRELIMINARY
Intelligent Systems
SCHEMATIC
ANALOG
2400, 3600 SERIES
102350
IP
D
9/19/82
ENGR. RELEASE
FOCUS ADJUST
G2 ADJUST
BRIGHTNESS
HIGH VOLTAGE ADJUST
VERTICAL CENTERING
VERTICAL DEFLECTION WINDING
HORIZ CENTERING
HORIZONTAL DEFLECTION WINDING
OVERCURRENT ADJUST
FAN
LINE SYNC
H SYNCBL
V SYNCBL
LVRAM
HSYNCBL
VSYNCBL


UA2
7445
UA4
7445
UA1
74LS03
SPACE BAR
ALPHA LOCK
COMMAND
SHIFT
CONTROL
REPEAT
RESET
BREAK
BLACK
INSERT CHAR
RED
DELETE LINE
GREEN
INSERT LINE
YELLOW
DELETE CHAR
BLUE
AUTO
MAGENTA
CYAN
WHITE
HOME
TAB
CURSOR →
CURSOR ↓
CURSOR ←
ESC
ERASE LINE
CURSOR ↑
ERASE PAGE
CARRIAGE RETURN
FORMS ON
AT ON
BACKARO ON
BLINK AT OFF
BLINK ON
NOTES:
KEYBOARD SCHEMATIC
101893
D
2

REVISIONS				
REV	DESCRIPTION	ECN	DATE	APPROVED
1	ENG. RELEASE	2947	2-25-83	DLT



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN Buton	10/27/82
CHECKED	
ENG David Trzeinski	1/13/83

PROPRIETARY

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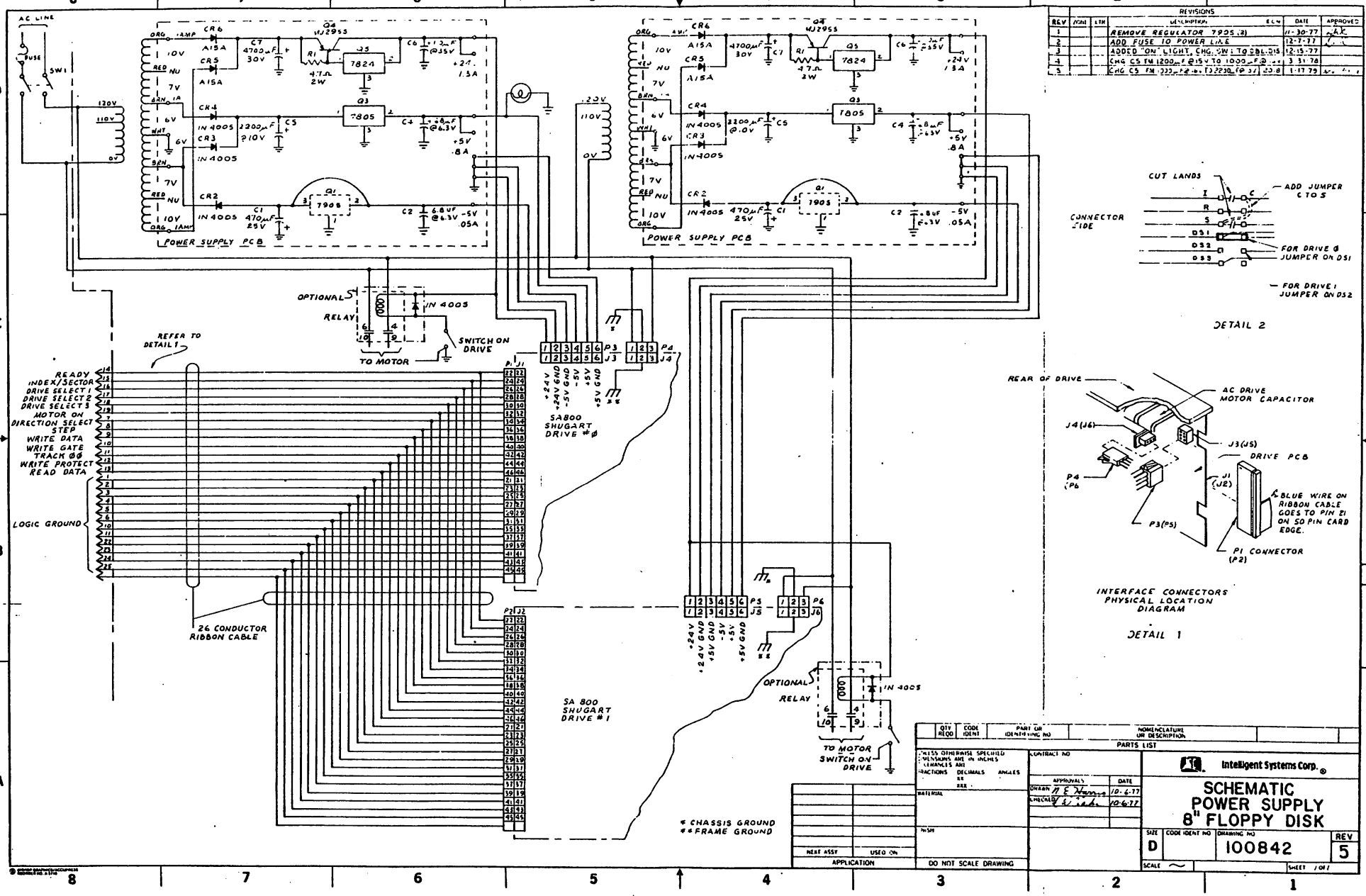
Intelligent Systems

SCHEMATIC
DISK DRIVE POWER SUPPLY

SIZE	DRAWING NO	REV
B	102362	1

SCALE N SHEET 1 OF 1



REVISIONS					
REV	ITEM	LTR	DESCRIPTION	DATE	APPROVED
1			REMOVE REGULATOR 7905 (2)	11-30-77	A.K.
2			ADD FUSE TO POWER LINE	12-7-77	
3			ADDED "ON" LIGHT, CHG. SW. TO DBL. DIS	12-15-77	
4			CHG C5 FM 1200μF @ 15V TO 1000μF @ 25V	3 31 78	
5			CHG C5 FM 2200μF @ 25V TO 2200μF @ 35V	1-17-79	

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCES ARE: FRACTIONS ±; DECIMALS .XX ±; .XXX ±; ANGLES ±

CONTRACT NO

APPROVALS	DATE
DRAWN	10-6-77
CHECKED	10-6-77

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

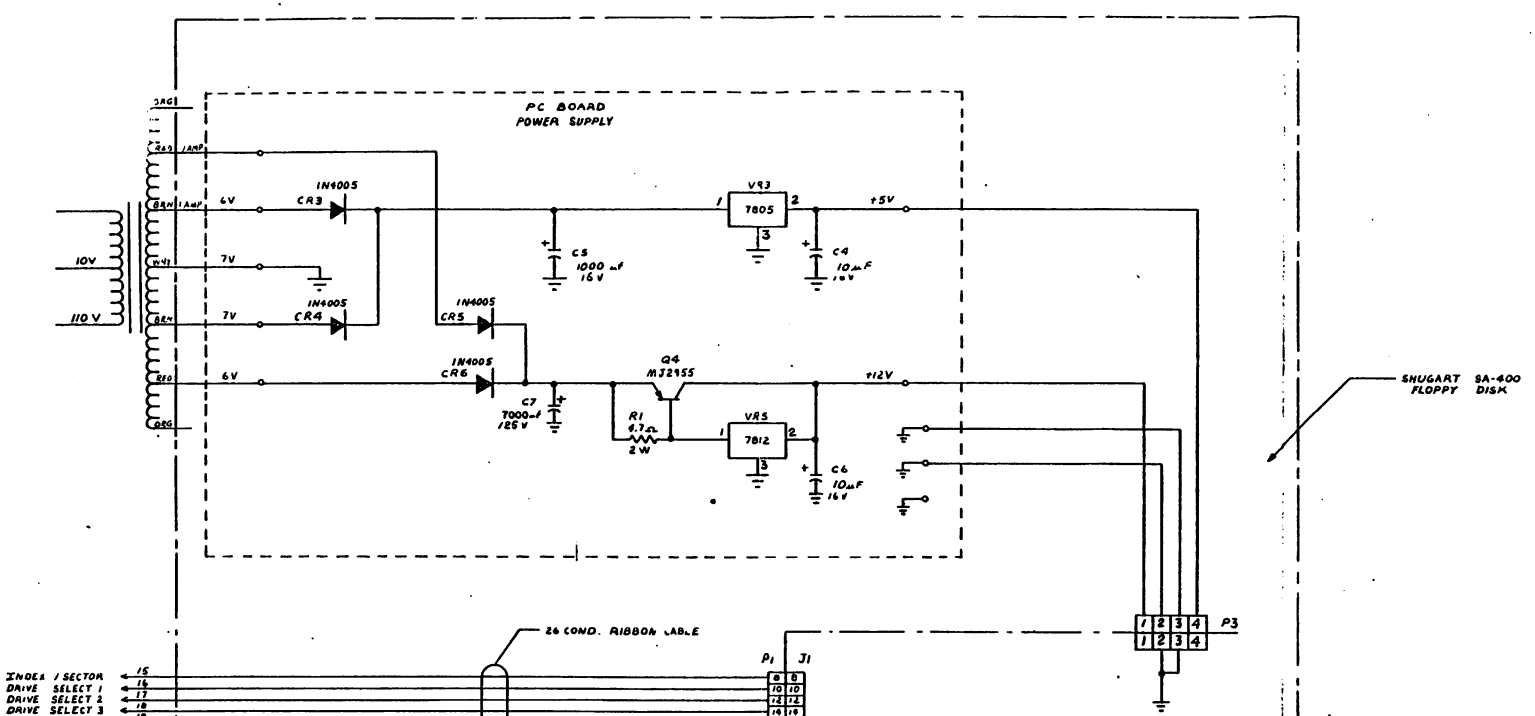
Intelligent Systems Corp.

SCHEMATIC POWER SUPPLY 8" FLOPPY DISK

SIZE	CODE IDENT NO	DRAWING NO	REV
D		100842	5

SCALE ~ SHEET 1 OF 1

REVISIONS						
REV	ZONE	LTR	DESCRIPTION	ECN	DATE	APPROVED
1			CHANGED 6.8 uF TO 33 uF		10-12-77	
2			CHG C5 .200 uF @ 5V TO 1000 uF @ 16V		3-31-78	
3			CHG C7 (WAS 8900 UF @ 25V)	2348	MH10 2083	



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
NEXT ASSY USED ON
APPLICATION
DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN Stanley Hazard	7-13-77
CHECKED	7-13-77

Intelligent Systems Corp.®

SCHEMATIC POWER SUPPLY SINGLE MINI DISK

SIZE	CODE IDENT NO	DRAWING NO	REV
D		100830	3

SCALE NONE SHEET 1 OF 1